

CURRICULUM VITAE

MAGNUS SJÄLANDER

PERSONAL INFORMATION

NAME **Magnus Sjölander**
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WORK EXPERIENCE

MARCH 2010 - **Chalmers University of Technology** **Post-Doctoral Position**
CURRENT Investigating power-aware management for LTE base-stations (collaboration with Ericsson). Implementation and parallelization of LTE uplink workload for scheduling and power optimization on Tiler TILEPro64 development board (64-core processor). Mentoring and co-supervising Ph.D. students, and supervising M.Sc. students.

JULY 2008 - **Aeroflex Gaisler** **Digital Design Engineer**
FEBRUARY 2010 Design of multi-core system on chips (SoC) for aerospace and the embedded domain, development of IP cores, development of the second generation of the GRLIB IP library, and writing research proposals.

APRIL 2003 - **Chalmers University of Technology** **Researcher & Teaching Assistant**
JUNE 2008 Research on flexible architectures, efficient multiplier circuits, and multi-core systems. Supervision of the final year project in VLSI design and several master thesis projects. Installed, maintained, and supported VLSI research group's EDA tool-flows.

AUGUST - **NXP Semiconductors** **Ph.D. Internship**
NOVEMBER 2007 Design and evaluation of a multi-core architecture based on scheduling units. The work resulted in patent application PCT/IB2009/051035 being filed at the European Patent Office.

AUGUST 2001 - **Luleå University of Technology** **Lab Assistant**
JUNE 2002 Lab assistant for beginner courses in Java programming.

AUGUST 1997 - **Palmcrantz High-school** **Systems Administrator**
AUGUST 1998 Maintenance and configuration of the schools Novell servers and Windows clients.

EDUCATION

APRIL 2006 - **Chalmers University of Technology** **Ph.D. in CE**
JUNE 2008 Doctor of Philosophy in Computer Engineering.
Thesis: "Efficient and Flexible Embedded Systems and Datapath Components".

APRIL 2003 - **Chalmers University of Technology** **Lic.Eng. in CE**
MARCH 2006 Licentiate of Engineering in Computer Engineering.
Thesis: "Efficient Reconfigurable Multipliers Based on the Twin-Precision Technique".

JULY 2000 - **Nanyang Technological University** **Exchange**
JUNE 2001 Exchange student at Nanyang Technological University, Singapore.

AUGUST 1998 - **Luleå University of Technology** **M.Sc. in CSE**
FEBRUARY 2003 Graduated with a Master of Science in Computer Science and Engineering.
Thesis: "Design and Implementation of a DDR SDRAM Controller for System on Chip".

PROFESSIONAL ACTIVITIES

INVITED TALKS

- Research presentation at Chinese Academy of Science, Beijing, China, 2011.
- Research presentation at IBM Research, Beijing, China, 2011.
- Research presentation at Swedish Tiler User's Group Workshop, Swedish Institute of Computer Science, Stockholm, Sweden, 2011.
- Invited lecturer for the "Methods for Electronic System Design and Verification" course, Chalmers University of Technology, Göteborg, Sweden, 2008 and 2009.
- Research presentation at NXP Semiconductors, Eindhoven, Netherlands, 2007.

- COMMISSIONS OF TRUST
- Program committee member of the International Conference on Supercomputing, 2011.
 - Organizer of Workshop on Emerging Supercomputing Technologies, 2011.
 - Reviewer, ACM Transactions on Architecture and Code Optimization, 2011.
 - Reviewer, IEEE Transactions on Very Large Scale Integration Systems, 2006-current.
 - Reviewer, Elsevier Journal of Systems Architecture, 2011-current.
 - Reviewer, IEEE International Conference on Very Large Scale Integration, 2011.
 - Reviewer, IEEE Transactions on Circuits and Systems-Part II, 2010.
 - Reviewer, IEEE International Conference on Electronics, Circuits, and Systems, 2009.

- EXTRACURRICULAR FUNCTIONS
- Ph.D. student representative on the Undergraduate Education Steering Group at Chalmers University of Technology, 2006-2007.
 - Ph.D. student representative on the Undergraduate Studies Board in Computer Science and Engineering at Chalmers University of Technology, 2005-2007.
 - Ph.D. student representative on the Department of Computer Science and Engineering Council at Chalmers University of Technology, 2004-2007.
 - Member of the Ph.D. Student Council at Chalmers University of Technology, 2004-2008.

- PUBLICATIONS
- Author of four peer-reviewed journal publications.
 - Author of 18 peer-reviewed conference publications.
 - Author of five peer-reviewed workshop publications.
 - Author of 14 technical publications.

PATENT Patent pending “Look-Ahead Task Management”, PCT/IB2009/051035 filed at the European Patent Office on March 12th, 2008.

- DEVELOPED SOFTWARE
- LTE Uplink Receiver PHY benchmark, <http://sourceforge.net/projects/lte-benchmark/>. A realistic parallel (POSIX threads) implementation of the baseband processing for an LTE mobile base station.
 - FlexSoc, <http://www.flexsoc.org>. A complete tool-suite for hardware/software design-space exploration of an exposed architecture. The suite consists of a compiler, simulator, and RTL generator. All the tools are integrated into a cohesive framework.
 - Multiplier generator, <http://www.sjalander.com/research/multiplier>. A publicly available VHDL generator for parallel multipliers.

- GRANTS AND AWARDS
- Ericsson collaboration grant (co-PI) with Sally A. McKee, 250 kSEK, 2011.
 - Knut and Alice Wallenberg Foundation, for attending the International Conference on Supercomputing and the Federated Computing Research Conference, 27 kSEK, 2011.
 - Knut and Alice Wallenberg Foundation, for attending the summer school on Advanced Computer Architecture and Compilation for Embedded Systems, 15.5 kSEK, 2010.
 - HiPEAC Internship Grant, NXP Semiconductors, Netherlands, 13 kEUR, 2007.
 - Scholarship from “Chalmersska Forskningsfonden”, Research affiliate at NXP Semiconductors, Netherlands, 23 kSEK, 2007.
 - HiPEAC 2007 Conference Grant, 250 EUR, 2007.

- PH.D. STUDENT SUPERVISION
- Actively mentoring and co-supervising Ph.D. students:
- Alen Bardizbanyan, together with Professor Per Larsson-Edefors.
 - Dmitry Knyagin, together with Docent Sally A. McKee.
 - Bhavishya Goel, together with Docent Sally A. McKee.
 - Tung Hoang Thanh, together with Professor Per Larsson-Edefors.

M.SC. THESIS SUPERVISION Supervised more than ten final year master thesis projects (30 or 60 ECTS) on the topic of hardware and software implementation of embedded systems, 2006-2011.

THESES

M. Sjölander, “**Efficient and Flexible Embedded Systems and Datapath Components**” *Thesis for the Degree of Doctor of Philosophy*, Chalmers University of Technology, June 2008, ISSN 0346-718X Technical Report 40D.

M. Sjölander, “**Efficient Reconfigurable Multipliers Based on the Twin-Precision Technique**” *Thesis for the Degree of Licentiate of Engineering*, Chalmers University of Technology, March 2006, ISSN 1652-876X Technical Report 12L.

M. Sjölander, “**Design and Implementation of a DDR SDRAM Controller for System on Chip**” *Thesis for the Degree of Master of Science*, Luleå University of Technology, February 2003, ISSN 1402-1617 NR 2003:038.

PUBLICATIONS

PEER-REVIEWED JOURNALS

T. Hoang-Thanh, M. Sjölander, and P. Larsson-Edefors, “**High-Speed, Energy-Efficient 2-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit**”, *IEEE Transactions on Circuits and Systems, I: Regular papers, Invited for SOCC Special Issue*, vol. 57, no. 12, pp. 3073-3081, Dec. 2010.

M. Thuresson, M. Sjölander, M. Björk, L. Svensson, P. Larsson-Edefors, and P. Stenström, “**FlexCore: Utilizing Exposed Datapath Control for Efficient Computing**”, *Journal of Signal Processing Systems*, vol. 57, no. 1, pp. 5-19, Oct. 2009.

M. Sjölander, and P. Larsson-Edefors, “**Multiplication Acceleration through Twin Precision**”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 9, pp. 1233-1246, Sep. 2009.

M. Islam, M. Sjölander, and P. Stenström, “**Early Detection and Bypassing of Trivial Operations to Improve Energy Efficiency of Processors**”, *Microprocessors and Microsystems, Elsevier*, vol. 42, no. 4, pp. 183-196, Nov. 2007.

PEER-REVIEWED CONFERENCES

M. Sjölander, S. A. McKee, P. Brauer, D. Engdal, and A. Vajda, “**An LTE Uplink Receiver PHY Benchmark and Subframe-Based Power Management**”, *To be presented at the IEEE International Symposium on Performance Analysis of Systems and Software*, New Brunswick, USA, pp. , 1-3 Apr. 2012.

S. Wong, A. Brandon, F. Anjam, R. Sedorf, R. Giorgi, Z. Yu, N. Puzovic, S. A. McKee, M. Sjölander, L. Carro, and G. Keramidis, “**Early Results From ERA Embedded Reconfigurable Architectures**”, *Proceedings of IEEE International Conference on Industrial Informatics*, Lisbon, Portugal, pp. 816-822, 26-29 Jul. 2011.

M. Sjölander, S. A. McKee, B. Goel, P. Brauer, D. Engdal, and A. Vajda, “**Power-Aware Resource Scheduling in Base Stations**”, *Proceedings of IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems*, Singapore, Singapore, pp. 462-465, 25-27 Jul. 2011.

K. Subramaniyan, E. Ryman, M. Sjölander, T. Hoang-Thanh, M. Islam, and P. Larsson-Edefors, “**FlexDEF: Development Framework for Processor Architecture Implementation and Evaluation**”, *Proceedings of Conference on Ph.D Research in Microelectronics and Electronics*, Trento, Italy, pp. 462-465, 3-7 Jul. 2011.

T. Hoang-Thanh, M. Sjölander, and P. Larsson-Edefors, “**High-Speed, Energy-Efficient 2-Cycle Multiply-Accumulate Architecture**”, *Proceedings of IEEE International SoC Conference*, Belfast, Northern Ireland, UK, pp. 119-122, 9-11 Sep. 2010.

T. Hoang-Thanh, U. Jälmlbrant, E. Hagopian, K. P. Subramaniyan, M. Sjölander and P. Larsson-Edefors, “**Design Space Exploration for an Embedded Processor with Flexible Datapath Interconnect**”, *Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors*, Rennes, France, pp. 55-62, 7-9 Jul. 2010.

P. Kimfors, N. Broman, A. Haraldsson, K. P. Subramaniyan, M. Sjölander, H. Eriksson, and P. Larsson-Edefors, “**Custom Layout Strategy for Rectangle-Shaped Log-Depth Multiplier Reduction Tree**”, *Proceedings of IEEE International Conference on Electronics, Circuits and Systems*, Hammamet, Tunisia, pp. 77-80, 13-16 Dec. 2009.

T. Hoang-Thanh, M. Själander, and P. Larsson-Edefors, “**Double Throughput Multiply-Accumulate Unit for FlexCore Processor Enhancements**”, *Proceedings of IEEE International Symposium on Parallel & Distributed Processing*, Rome, Italy, pp. 1-7, 25-26 May 2009.

T. Schilling, M. Själander, P. Larsson-Edefors, “**Scheduling for an Embedded Architecture with a Flexible Datapath**”, *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, Tampa, Florida, pp. 151-156, 13-15 May 2009.

M. Thuresson, M. Själander, and P. Stenström, “**A Flexible Code-Compression Scheme using Partitioned Look-Up Tables**”, *Proceedings of 4th International Conference on High-Performance and Embedded Architectures and Compilers*, Paphos, Cyprus, pp. 95-109, 25-28 Jan. 2009.

M. Själander, A. Terechko, M. Duranton, “**A Look-Ahead Task Management Unit for Embedded Multi-Core Architectures**”, *Proceedings of Euromicro Conference on Digital System Design: Architectures, Methods, and Tools*, Parma, Italy, pp. 149-157, 3-5 Sep. 2008.

M. Själander, and P. Larsson-Edefors, “**High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree**”, *Proceedings of IEEE International Conference on Electronics, Circuits and Systems*, St. Julian’s, Malta, pp. 33-36, 1-3 Sep. 2008.

M. Thuresson, M. Själander, M. Björk, L. Svensson, P. Larsson-Edefors, and P. Stenström, “**FlexCore: Utilizing Exposed Datapath Control for Efficient Computing**”, *Proceedings of IEEE International Symposium on Systems, Architectures, Modeling and Simulation*, Samos, Greece, pp. 18-25, 16-19 Jul. 2007.

M. Själander, P. Larsson-Edefors, and M. Björk, “**A Flexible Datapath Interconnect for Embedded Applications**”, *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, Porto Alegre, Brazil, pp. 15-20, 9-11 May. 2007.

H. Eriksson, P. Larsson-Edefors, M. Sheeran, M. Själander, D. Johansson, M. Schölin, “**Multiplier Reduction Tree with Logarithmic Logic Depth and Regular Connectivity**”, *Proceedings of IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, pp. 15-20, 21-24 May. 2006.

M. Själander, M. Drazdziulis, P. Larsson-Edefors, and H. Eriksson, “**A Low-Leakage Twin-Precision Multiplier Using Reconfigurable Power Gating**”, *Proceedings of IEEE International Symposium on Circuits and Systems*, Kobe, Japan, pp. 1654-1657, 23-26 May 2005.

M. Själander, H. Eriksson, P. Larsson-Edefors, “**An Efficient Twin-Precision Multiplier**”, *Proceedings of IEEE International Conference on Computer Design*, San Jose, California, pp. 30-33, 10-13 Oct. 2004.

PEER-REVIEWED
WORKSHOPS

M. Själander, S. A. McKee, B. Goel, P. Brauer, D. Engdal, and A. Vajda, “**Power-Aware Resource Management for LTE Base Stations**”, *First International Software Technology Exchange Workshop*, Stockholm, Sweden, pp. 30-33, Nov. 2011.

G. Goumas, S. A. McKee, M. Själander, T. R. Gross, S. Karlsson, and L. Zhang, “**Adapt or Become Extinct!**”, *Proceedings of IEEE International Workshop on Adaptive Self-Tuning Computing Systems for the Exaflop Era*, San Jose, California, USA, pp. 30-33, 5 Jun. 2011.

A. Bardizbanyan M. Själander, and P. Larsson-Edefors, “**Reconfigurable Instruction Decoding for a Wide-Control-Word Processor**”, *Proceedings of IEEE International Reconfigurable Architectures Workshop*, Anchorage, Alaska, USA, pp. 30-33, 16-17 May 2011.

M. Andersson, L. Svensson, M. Själander, S. A. McKee, E. Catovic and P. Ingelhart, “**Yield Optimization Using Redundant Cores**”, *Third Swedish Workshop on Multi-Core Computing*, Göteborg, Sweden, pp. 30-33, Oct. 2010.

- M. Björk, M. Själander, L. Svensson, M. Thuresson, J. Hughes, M. Sheeran, K. Jeppson, J. Karlsson, P. Larsson-Edefors, and P. Stenström, “**Exposed Datapath for Efficient Computing**”, *Proceedings of HiPEAC Workshop on Reconfigurable Computing*, Ghent, Belgium, pp. 30-33, 28-30 Jan. 2007.
- TECHNICAL REPORTS N. Frolov, M. Själander, P. Larsson-Edefors, and Sally A. McKee, “**A SAT-Based Compiler for FlexCore**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:11-04, Apr. 2011.
- M. Själander, S. A. McKee, B. Goel, P. Brauer, D. Engdal, and A. Vajda, , “**Resource Management for an LTE Baseband Workload**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:11-05, Apr. 2011.
- B. Goel, M. Själander, S. A. McKee, V. Spiliopoulos, G. Keramidas, S. Kaxiras and K. Efstathiou, “**Infrastructures for Measuring Power**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:11-06, Apr. 2011.
- E. Ryman, K. P. Subramaniyan, T. Hoang-Thanh, M. Islam, M. Själander, and P. Larsson-Edefors, “**FlexTools: Design Space Exploration Tool Chain from C to Physical Implementation**”, *CDNLive! EMEA*, Munich, Germany, pp. 30-33, 4-6 May 2010.
- J. Andersson, M. Själander, J. Gaisler, and R. Weigand, “**Next Generation Multi-Purpose Microprocessor**”, *Data Systems In Aerospace*, Budapest, Hungary, pp. 30-33, 1-4 Jun. 2010.
- M. Själander, S. Habinc, and J. Gaisler, “**LEON4 Fourth Generation of the LEON Processor**”, *Data Systems in Aerospace*, Istanbul, Turkey, pp. 30-33, 26-29 May 2009.
- T. Hoang-Thanh, M. Själander, and P. Larsson-Edefors, “**Ultra-Low-Power 2-Cycle Multiply-Accumulate Architecture**”, *Swedish System-on-Chip Conference*, Arild, Sweden, pp. 30-33, 4-5 May 2009.
- U. Jälmbrent, E. Hagopian, M. Själander, and P. Larsson-Edefors, “**Design-Time Scheduling for Processor Exploration**”, *Swedish System-on-Chip Conference*, Arild, Sweden, pp. 30-33, 4-5 May 2009.
- T. Hoang-Thanh, M. Själander, and P. Larsson-Edefors, “**Double Throughput MAC for Performance Enhancement of the FlexCore Processor**”, *Swedish System-on-Chip Conference*, Gnesta, Sweden, pp. 30-33, 5-6 May 2008.
- M. Själander, and P. Larsson-Edefors, “**The Case for HPM-Based Baugh-Wooley Multipliers**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:08-8, 2008.
- M. Thuresson, M. Själander, P. Stenström, “**A Flexible Code Compression Scheme using Partitioned Look-Up Tables**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:08-15, 2008.
- M. Björk, M. Själander, L. Svensson, M. Thuresson, J. Hughes, K. Jeppson, J. Karlsson, P. Larsson-Edefors, M. Sheeran, and P. Stenström, “**Exposed Datapath for Efficient Computing**”, *Technical report - Department of Computer Science and Engineering, Chalmers University of Technology and Göteborg University*, ISSN: 1652-926X, No:06-21, 2006.
- M. Brinck, K. Eklund, M. Själander, and P. Larsson-Edefors, “**An Efficient FFT Engine Based on Twin-Precision Computation**”, *Swedish System-on-Chip Conference*, Kålmorden, Sweden, pp. 30-33, 4-5 May 2006.
- M. Själander and P. Larsson-Edefors, “**A Power-Efficient and Versatile Modified-Booth Multiplier**”, *Swedish System-on-Chip Conference*, Tammsvik, Sweden, pp. 30-33, 18-19 Apr. 2005.