

**PERSONAL INFORMATION**

NAME Magnus Själander  
 ADDRESS Droningens Gate 14, 7011 Trondheim, Norway  
 EMAIL magnus.sjalander@ntnu.edu

**EDUCATION**

NOVEMBER 2019 **Docent in Computer Science** **Uppsala University**  
 Docent Lecture: “Past and Current Trends in Computer Architecture”.

JUNE 2008 **Ph.D. in Computer Engineering** **Chalmers University of Technology**  
 Thesis: “Efficient and Flexible Embedded Systems and Datapath Components”.  
 Designed the microarchitecture of a novel, embedded processor core that exposes the entire datapath to the compiler. The richer hardware/software interface makes it possible to explicitly manage hardware resources and enables new compiler optimizations.

MARCH 2006 **Lic.Eng. in Computer Engineering** **Chalmers University of Technology**  
 Thesis: “Efficient Reconfigurable Multipliers Based on the Twin-Precision Technique”.  
 Designed circuit techniques for high-performance, low-power parallel multipliers.

FEBRUARY 2003 **M.Sc. in Computer Science and Engineering** **Luleå University of Technology**  
 Thesis: “Design and Implementation of a DDR SDRAM Controller for System on Chip”.  
 Designed an ASIC memory controller as part of an implementability study to help Ericsson AB choose their next-generation memory technology.

JULY 2000 - **Exchange Student** **Nanyang Technological University**  
 JUNE 2001 International exchange student at the school of Computer Engineering and the school of Electrical & Electronic Engineering, Nanyang Technological University, Singapore.

**RESEARCH AND INDUSTRIAL EXPERIENCE**

JANUARY 2016 - **Associate Professor—Computer Architecture** **NTNU**  
 PRESENT Focus on energy efficient computing and hardware/software interaction.  
 Coordinator of the Energy Efficient Computing Systems (EECS) strategic research area.

JUNE 2016 - **Visiting Senior Lecturer—Computer Security** **Uppsala University**  
 PRESENT Investigating methods to mitigate speculative side-channel attacks.

MARCH 2014 - **Research Associate—Emerging Technologies** **Uppsala University**  
 DECEMBER 2015 Investigated emerging technologies, e.g., single atom transistors, and their potential use for future high-performance and energy-efficient architectural designs.

JULY 2012 - **Research Scientist—Energy-Efficient Computing** **Florida State University**  
 DECEMBER 2013 Investigated architectural and compiler techniques for energy-efficient processors and memory systems. Reassessed conventional hardware/software interfaces to convey more information from the application to the hardware. Mentored and co-supervising Ph.D. students.

MARCH 2010 - **Postdoctoral Scholar** **Chalmers University of Technology**  
 MARCH 2012 Investigated power-aware management for LTE base stations (collaboration with Ericsson AB). Implementation and parallelization of LTE uplink workload for scheduling and power optimization on Tiler TILEPro64 development board (64-core processor). Mentored and co-supervised Ph.D. students, and supervised M.Sc. thesis students.

JULY 2008 - **Digital Design Engineer** **Aeroflex Gaisler**  
 FEBRUARY 2010 Designed multi-core system on chips (SoCs) for aerospace and the embedded domain, developed IP cores, and a prototype of the second generation of the GRLIB IP library.

APRIL 2003 - **Research & Teaching Assistant** **Chalmers University of Technology**  
 JUNE 2008 Researched on flexible architectures, efficient multiplier circuits, and multi-core systems. Supervised the final year project course in VLSI design and M.Sc. thesis students. Installed, maintained, and supported the VLSI research group’s EDA ASIC tool-flows.

AUGUST - **Visiting Researcher** **NXP Semiconductors**  
 NOVEMBER 2007 Designed and evaluated a multi-core architecture based on scheduling units. The work resulted in patent application PCT/IB2009/051035 being filed at the European Patent Office.

**PROFESSIONAL ACTIVITIES**

**PUBLICATIONS** Author of more than 50 internationally peer-reviewed articles and published in tier-1 venues for Computer Architecture (ISCA, HPCA, PACT, IEEE TC), Optimizing Compilers (PLDI, CGO, ACM TACO), and Digital Design (FPL, DATE, ACM TRETTS, IEEE TVLSI).  
H-index: 18, Citations: 1008 according to Google Scholar on 2021-06-21.

- Author of one book and one book chapter.
- Author of 12 peer-reviewed journal articles.
- Author of 37 peer-reviewed conference articles.
- Author of nine peer-reviewed workshop and poster articles.
- Author of 17 other publications.

**NB!** Conferences are the premier venue for the fields of Computer Architecture, Optimizing Compilers, and Digital Design with the top-tier conferences being much more prestigious than journals in the same field.

- PATENTS**
- “Systems and methods for invisible speculative execution”, C. Sakalis, S. Kaxiras, A. Ros, A. Jimborean, M. Själander, US Patent App. 16/825,399.
  - “Modulated Approximation in Logic Circuits”, G.-Z. M. Fernando, S. Kaxiras, and M. Själander, EP3246814A1, 16 May, 2016.
  - “Data Filter Cache Designs for Enhancing Energy Efficiency and Performance in Computing Systems”, D. Whalley, M. Själander, A. Bardizbanyan, and P. Larsson-Edefors, US9612960 B2, 19 Nov. 2012.
  - “Systems and Methods for Improving Processor Efficiency Through Caching”, D. Whalley, M. Själander, A. Bardizbanyan, P. Larsson-Edefors, and P. Gavin, US9600418 B2, 19 Nov. 2013.
  - “Look-Ahead Task Management”, A. Terechko, G. Al-Kadi, M. Duranton, and M. Själander, PCT/IB2009/051035, 12 Mar. 2008.

- AWARDS AND RECOGNITIONS**
- ACM Senior Member, December 2020.
  - HiPEAC 2020 Paper Award—“Twig: Multi-Agent Task Management for Colocated Latency-Critical Cloud Services”, *ACM International Conference on High-Performance Computer Architecture (HPCA)*, 2020.
  - HiPEAC 2019 Paper Award—“Efficient Invisible Speculative Execution to Improve Energy Efficiency of Processors”, *ACM/IEEE International Symposium on Computer Architecture (ISCA)*, 2019.
  - One out of five nominees for the best paper award—“BISMO: A Scalable Bit-Serial Matrix Multiplication Overlay for Reconfigurable Computing”, *IEEE International Conference on Field-Programmable Logic and Applications (FPL)*, 2018.
  - HiPEAC 2018 Paper Award—“SWOOP: Software-Hardware Co-Design for Non-Speculative, Execute-Ahead, In-Order Cores”, *ACM International Conference on Programming Language Design and Implementation (PLDI)*, 2018.
  - Paper of the month—“Static Instruction Scheduling for High Performance on Limited Hardware”, *IEEE Transactions on Computers*, April 2018.
  - Best of CAL—“Transcending Hardware Limits with Software Out-of-order Processing”, *IEEE Computer Architecture Letters*, 2017.
  - Member of HiPEAC, 28 Apr. 2017.
  - Senior Member of IEEE, 7 Feb. 2015.
  - One out of four nominees for best paper award—“An LTE Uplink Receiver PHY Benchmark and Subframe-Based Power Management”, *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2012.

- GRANTS
- EU Horizon 2020, Marie Skłodowska-Curie Individual Fellowship, host for Shounak Chakraborty, “Towards Employing Compilers for Thermal Management and Optimal Data Placement in Hybrid Caches”, 214k Euro, 2021-2022. Grant Agreement No: 898296.
  - NTNU Enabling Technologies, “CODE — Future High-Performance Processors Through Software-Hardware CO-DEsign”, approximately 3M NOK, 2020-2024.
  - Norwegian Research Council (NFR), Young Research Talents, co-PI with Project Manager Rakesh Kumar, “TailorMade: Tailoring Server Processors to Application Characteristics for Sustainable Warehouse-Scale Computing”, 8M NOK, 2020-2024.
  - EU Horizon 2020, FET-Open, Work Package Leader, “SpinENGINE: Harnessing the Emergent Properties of Nanomagnet Ensembles for Massively Parallel Data Analysis”, 3M Euro (NTNU: 831.5k), 2020-2024. Grant Agreement No: 861618.
  - EU Horizon 2020, Digital Innovation Hubs and Platforms, Principal Investigator, “BOWI: Boosting Widening Digital Innovation Hubs”, 7.9M Euro (NTNU: 285k), 2020-2023. Grant Agreement No: 873155.
  - Norwegian Research Council (NFR), IKTPLUSS, Gunnar Tufte, Erik Folven, Magnus Själander, Nichele Stefano, and Ioanna Sandvig, “SOCRATES: Self-Organizing Computational substRATES—Phase II”, 15.5M NOK, 2018-2022. Grant Agreement No: 270961.
  - NTNU H2020 Goldcard, “Energy Efficient Computing Systems”, Magnus Själander and Per Gunnar Kjeldsberg, 2M NOK, 2017-2019.
  - NTNU Infrastructure, “Energy efficient high Performance computing research Infrastruc-ture (EPIC)”, Magnus Jahre, Magnus Själander, and Frank Lindseth, 3M NOK, 2017.
  - Norwegian Research Council (NFR), IKTPLUSS, Gunnar Tufte, Erik, Folven, Magnus Själander, Nichele Stefano, and Ioanna Sandvig, “SOCRATES: Self-Organizing Computa-tional substRATES—Phase I”, 500k NOK, 2017.
  - Swedish Research Council (VR), Project Research Grant for Young Scientists, “Leveraging Multi-Value Logic to Modulate Approximation for Future Nano Devices”, 3.4M SEK, 2016-2019. Grant Agreement No: 2015-05159.
  - National Science Foundation (NSF), International Research Experience for Students (IRES) Award (NSF:1358147), 250k USD, 2015-2017. (Submitted as a co-PI together with Gary Tyson, An-I Wang, and David Whalley while at FSU)

- COMMISSIONS  
OF TRUST
- **Faculty board member** at the Faculty of Information Technology and Electrical Engi-neering, NTNU, 2021-present.
  - **Coordinator of the Energy Efficient Computing Systems (EECS) strategic research area** at NTNU, 2017-present.
  - **Head of the Computing research unit** at the Department of Computer Science, NTNU, 2018-2021.
  - Employee representative in the assessment board for the Head of Department, Computer Science, NTNU, 2021.
  - Assessment board member for Associate Professor/Professor position in Algorithms and Complexity, NTNU, 2020.
  - Assessment Committee member, candidate evaluation for Postdoc position in biometrics for the EU D4FLY project, NTNU, 2019.
  - Expert Committee member, candidate evaluation for Associate Professor position in Com-piler Design, NTNU, 2019.
  - Deputy head of the Computing research group at the Department of Computer Science, NTNU, 2017.
  - Deputy head of the Computer Architecture Design (CARD) research group at the De-partment of Computer Science, NTNU, 2016.
  - Expert Committee member, candidate evaluation for Tenure Track position in Energy Efficient Computing, NTNU, 2017.
  - Program Chair of Nordic Workshop on Multi-Core Computing, 2016.
  - Board member, Uppsala Fotografiska Sällskap, 2015.
  - Board member, Housing association Ymergården, 2014-2015.

- ORGANIZATION OF EVENTS
- Publication Chair of the IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022
  - Publication Chair of the ACM International Conference on Computing Frontiers (CF), 2017.
  - Organizer of Energy Efficient Computing Systems Seminar, 2017.
  - Organizer of the Nordic Workshop on Multi-Core Computing (MCC), 2016.
  - Organizer of Workshop on Emerging Supercomputing Technologies (WEST), 2011.
- PROGRAM COMMITTEES
- IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022.
  - IEEE Nordic Circuits and Systems Conference (NorCAS), 2021.
  - IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE), 2021-2019.
  - ACM International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 2021-2017.
  - ACM International Conference on Computing Frontiers (CF), 2020-2018 and 2016-2014.
  - Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP), 2021, 2020, and 2014.
  - Nordic Workshop on Multi-Core Computing (MCC), 2019-2015.
  - IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2019.
  - International Symposium on Advanced Parallel Processing Technology (APPT), 2019.
  - International Workshop on Programmability and Architectures for Heterogeneous Multi-cores (MULTIPROG), 2017.
  - IEEE International Conference on Networking, Architecture, and Storage (NAS), 2015-2014
  - ACM International Conference on Languages, Compilers and Tools for Embedded Systems (LCTES), 2014.
  - International Workshop on New Algorithms and Programming Models for the Manycore Era (APMM), 2014.
  - ACM International Conference on Supercomputing (ISC), 2011.
- REVIEWER
- ACM Computing Surveys (CSUR), 2020.
  - Springer International Journal of Parallel Programming (IJPP), 2020.
  - IEEE Access, 2020.
  - ACM Transactions on Reconfigurable Technologies and Systems (TRETTS), 2020.
  - IEEE Transactions on Computer Architecture Letters (CAL), 2019.
  - IEEE Transactions on Computers (TC), 2019.
  - IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2006-2016.
  - Elsevier Parallel Computing Journal, 2016.
  - Elsevier Microprocessors and Microsystems Journal, 2016.
  - Elsevier Microelectronics Journal, 2015.
  - ACM Transactions on Architecture and Code Optimization (TACO), 2011-2015.
  - Springer The Journal of Signal Processing Systems, 2014.
  - ACM Transactions on Embedded Computing Systems, 2014.
  - IEEE Transactions on Circuits and Systems-Part II, 2010, 2014.
  - Elsevier Journal of Systems Architecture, 2011-2012.
  - IEEE International Conference on Very Large Scale Integration, 2011.
  - IEEE International Conference on Electronics, Circuits, and Systems, 2009.

- INVITED TALKS
- “How Can We Make Digital Technology Sustainable?”, Elements of AI webinar on Artificial Intelligence for a Better World, 2021.
  - “BISMO: A Scalable Bit-Serial Matrix Multiplication Overlay for Reconfigurable Computing”, FPGA forum, Trondheim, Norway, 2020.
  - “Time to Challenge Established Assumptions and Methods”, Ericsson, Sweden, 2018.
  - “Hardware-Software Codesign for Efficiency Computing”, Seminar on Advances in Heterogeneous Computing from Hardware to Software, Shonan Village Center, Japan, 2018.
  - “Modulated Approximation”, Workshop at ISPASS: Benchmarking and Measuring Approximate Computing, Uppsala, Sweden, 2016.
  - “Approximate Computing in the Advent of Emerging Multi-Value Devices”, Norwegian University of Science and Technology, Trondheim, Norway, 2015.
  - “Exploiting Semantic Information to Achieve High Efficiency Computing”, Nanyang Technological University, Singapore, 2013.
  - “Power-Aware Resource Management for LTE Base Stations”, Uppsala University, Uppsala, Sweden, 2013.
  - “Improving Data Access Efficiency by Using a Tagless Access Buffer”, Michigan Technological University, Houghton, Michigan, USA, 2013.
  - “The Importance of a Toolchain”, Ericsson AB, Göteborg, Sweden, 2012.
  - “From Arithmetic Circuits to System on Chips”, ARM Ltd., Trondheim, Norway, 2012.
  - “Power-Aware Scheduling and Low-Power Architectures”, Florida State University, Tallahassee, Florida, USA, 2012.
  - “Power-Aware Scheduling for LTE Mobile Base-Stations”, Chinese Academy of Science, Beijing, China, 2011.
  - “Power-Aware Scheduling for LTE Mobile Base-Stations”, IBM Research, Beijing, China, 2011.
  - “An LTE Benchmark on Tilera and Power Measurements”, Swedish Tilera User’s Group Workshop, Swedish Institute of Computer Science, Stockholm, Sweden, 2011.
  - Invited lecturer for the course, “Methods for Electronic System Design and Verification”, Chalmers University of Technology, Göteborg, Sweden, 2008 and 2009.
  - “FlexCore: An Exposed Datapath Architecture”, NXP Semiconductors, Eindhoven, Netherlands, 2007.

- PHD/LIC DEGREE EVALUATION
- Discussion leader (opponent), Licentiate of Mehrzad Nejat, Chalmers University of Technology, 2019.
  - External evaluator, Ph.D. thesis of Debasish Mukherjee, Indian Institute of Technology (Indian School of Mines), Dhanbad, 2019.
  - Assessment Committee member, Ph.D. defence of Yaman Umuroglu, Norwegian University of Science and Technology (NTNU), 2018.
  - Assessment Committee member, Ph.D. defence of Odd Rune Strømme Lykkebø, Norwegian University of Science and Technology (NTNU), 2017.
  - Assessment Committee member, Ph.D. thesis of Laust Brock-Nannestad, Technical University of Denmark (DTU), 2016.

- EXTRACURRICULAR FUNCTIONS
- Ph.D. student representative to the Undergraduate Education Steering Group at Chalmers University of Technology, 2006-2007.
  - Ph.D. student representative to the Evaluation Committee for Head of the Department of Computer Science and Engineering at Chalmers University of Technology, 2006.
  - Ph.D. student representative to the Undergraduate Studies Board in Computer Science and Engineering at Chalmers University of Technology, 2005-2007.
  - Ph.D. student representative to the Department of Computer Science and Engineering Council at Chalmers University of Technology, 2004-2007.
  - Member of the Ph.D. Student Council at Chalmers University of Technology, 2004-2008.
  - Member of the Embedded Electronic System Design master program’s curriculum committee at Chalmers University of Technology, 2007-2008 and 2010-2011.

**SUPERVISION AND MENTORING**

POSTDOCS Actively mentored and supervised two Postdocs.

- Shounak Chakraborty, NTNU, 2019-present.
- Rajiv Nishtala, NTNU, 2018-2020.

PH.D. STUDENTS Actively mentored and supervised 17 Ph.D. students.

- David Metz, main supervisor, NTNU, 2020-present.
- Amund Bergland Kvalsvik, main supervisor, NTNU, 2020-present.
- Anders Knap Gaustad, main supervisor, NTNU, 2020-present.
- Halvard Hummel, co-supervisor with Prof. Magnus Lie Hetland, NTNU, 2020-present.
- Lasse Agentoft Eggen, co-supervisor with Prof. Magnus Jahre, NTNU, 2020-present.
- Fatemeh Ghasemisoumeeh, co-supervisor with Prof. Magnus Jahre, NTNU 2020-present.
- Joseph Rogers, co-supervisor with Prof. Magnus Jahre, NTNU, 2020-present.
- Truls Asheim, co-supervisor with Prof. Rakesh Kumar, NTNU, 2019-present.
- Anders Strømberg, co-supervisor with Prof. Erik Folven, NTNU, 2019-present.
- Lahiru Rasnayake, main supervisor, NTNU, 2017-present.
- Chris Sakalis, main supervisor, Uppsala University, 2017-present.
- Nico Reissmann, mentored, NTNU, 2017-2019.
- Alen Bardizbanyan, co-supervisor with Prof. Per Larsson-Edefors, Chalmers, 2010-2013.
- Peter Gavin, mentored with Prof. David Whalley, Chalmers, 2011-2013.
- Bhavishya Goel, mentored with Docent Sally A. McKee, Chalmers, 2011-2012.
- Dmitry Knyagin, mentored with Docent Sally A. McKee, Chalmers, 2010-2012.
- Tung Hoang Thanh, mentored with Prof. Per Larsson-Edefors, Chalmers, 2008-2010.

M.SC. THESES Supervised 23 thesis projects on topics of hardware and software design and implementation.

- David Metz and Erling Jellum “Efficient Instruction Scheduling”, NTNU, 2020.
- Khakim Akhunov, “Way-predictive instruction cache access in Rocket Chip processor with RISC-V ISA”, NTNU 2020.
- Valentin Plotkin, “Evaluation of an Efficient Data Filter Cache in a RISC-V core”, NTNU, 2020.
- Edgar Mo Vedvik, “Implementing a RISC and L1 Data Cache in Hardware to Evaluate DAGDA Energy Efficiency”, NTNU, 2019.
- Ludvig Jordet, “Creation of a Software Programmable Hardware Interface”, NTNU, 2019.
- Kristoffer Monsen, “Challenges in Constructing a RISC-V Computing Platform”, NTNU, 2019.
- Martin Gundersen, “Analyzing an FPGA Neural Network Accelerator Design for Implementation in an ASIC”, NTNU, 2019.
- Erlend Sveen, “Strict Memory Protection for Microcontrollers”, NTNU, 2019.
- Håvard Tollefsen, “Evaluating performance impact of performing computations on storage nodes”, NTNU, 2018.
- Salahuddin Asjad, “Energy Efficient Data Accesses”, NTNU, 2017.
- Henrik Grandin, “Impact of Approximate Data in Arithmetic Operations”, Uppsala University, 2015.
- Gustaf Borgström, “Approximate computing for emerging technologies”, Uppsala University, 2015.
- Vahid Saljooghi, “Development and Integration of Level-1 Cache RTL Model”, Chalmers, 2012.
- Kashan Khurshid Ansari, “Microcode Optimization in FlexCore Compiler”, Chalmers, 2012.
- Hao Li, “A Cilk implementation of LTE Base-Station Uplink on TILEPro64”, Chalmers, 2012.
- Recep Gökhan Aslan and Cemil Caglar Boke, “DAT095 Project Renewal - Implementation of MP3 Player on FPGA”, Chalmers, 2011.
- Nikita Frolov, “Bau: A Declarative Scheduling Library”, Chalmers, 2011.

- M.Sc. THESES (CONTINUED)
- Johan Rydh, “Embedded Camera Remote Control”, Chalmers, 2011.
  - Ulf Jälmlbrant and Erik der Hagopian, “Improved configurability with FlexSoC For the purpose of design time scheduling for processor exploration”, Chalmers, 2009.
  - Thomas Schilling, “Scheduling Techniques for FlexCore”, Chalmers, 2008.
  - Abdifatah Farah, “Efficient Datapath Multipliers”, Chalmers, 2008.
  - Jonas Karlsson, “A MIPS and NISC implementation”, Chalmers, 2008.
  - Erik Ryman, “FlexCore implementation on FPGA”, Chalmers, 2007.
  - Martin Brink and Kristian Eklund, “A Flexible FFT/DCT Engine Using the Twin-Precision Technique”, 2006.
  - Jan Mårts and Tomas Carlqvist, “A Hardware Audio Decoder Using Flexible Datapaths”, 2006.

- RESEARCHERS
- Actively supervised five Researcher Assistants.
- Amund Bergland Kvalsvik, NTNU, 2020.
  - Fatemeh Ghasemisoumeeh, NTNU, 2018-2020.
  - Carlos Sanchez, Florida State University, 2013-2014.
  - Ryan Baird, Florida State University, 2013.
  - Brandon Davis, Florida State University, 2012-2013.

## PEDAGOGICAL EXPERIENCE

- TEACHING EXPERIENCE
- DT8123 PhD course in Advance Computing, NTNU, Spring 2021. Lecturer
  - TDT4260 Computer Architecture, NTNU, Spring 2016-2021. Examiner
  - TDT01 Architecture of Computing Systems, NTNU, Autumn 2018-2021. Lecturer
  - IDT109 Accelerating Systems with Programmable Logic Components, Uppsala University, Spring 2019. Guest Lecture
  - TDT01 Architecture of Computing Systems, Autumn 2017. Examiner
  - TDT4258 Low-Level Programming, NTNU, Autumn 2016 and 2017. Coordinator
  - IDT093 Computer Architecture, Uppsala University, Q4 2015. Instructor
  - Ph.D. course, EEC14 Energy Efficient Computing, Uppsala University, 2014. Examiner
  - DAT096 Embedded system design project, Chalmers University of Technology, Q3 2012. Project and curriculum development
  - Ph.D. course, Embedded Processor Implementation and Verification, Chalmers University of Technology, Q2-Q3 2010/2011. Instructor
  - EDA445 VLSI project course, Chalmers University of Technology, Spring 2004-2007. Instructor / Teaching assistant
  - EME010 Digital VLSI Design, Chalmers University of Technology, Q1 2003-2004. Teaching assistant
  - EDA455 System on Chip, Chalmers University of Technology, Q4 2004. Course development
  - EDA330/440 Computer System Engineering, Chalmers University of Technology, Q3 2004. Teaching assistant
  - SMD038 Imperative Programming, Luleå University of Technology, Q2 2001. Lab assistant

- PEDAGOGICAL TRAINING
- Supervising Students, Uppsala University, (2 weeks), 2015.
  - Supervising PhD Students, Uppsala University, (3 weeks), 2014.
  - Academic Teacher Training Course, Uppsala University, (5 weeks), 2014.
  - Quality and Standards in Thesis Work, Workshop, Uppsala University, 2014

## PUBLICATIONS

*Authors in italic are Postdocs, Ph.D., M.Sc., or B.Sc. students that I have supervised.*

- THESES
- M. Själander, “**Efficient and Flexible Embedded Systems and Datapath Components**”, *Doctor or Philosophy*, Chalmers University of Technology, June 2008, ISSN: 0346-718X, ISBN: 978-91-7385-137-4.

M. Själander, “**Efficient Reconfigurable Multipliers Based on the Twin-Precision Technique**”, *Licentiate of Engineering*, Chalmers University of Technology, Mar. 2006, ISSN: 1652-876X.

M. Själander, “**Design and Implementation of a DDR SDRAM Controller for System on Chip**”, *Master of Science*, Luleå University of Technology, Feb. 2003, ISSN: 1402-1617 NR 2003:038.

BOOKS AND  
CHAPTERS

M. Själander, M. Martonosi, and S. Kaxiras, “**Power-Efficient Computer Architectures: Recent Advances**”, *Synthesis Lectures on Computer Architecture*, Morgan & Claypool, Dec. 2014, ISBN: 978-1-62705-645-8.

B. Goel, S. A. McKee, and M. Själander, “**Techniques to Measurement, Model, and Manage Power**”, *Elsevier Advances in Computers, Green and Sustainable Computing: Part I*, vol. 87, pp. 7-54, Nov. 2012, ISBN: 978-0-12-396528-8 .

PEER-REVIEWED  
JOURNALS

C. Sakalis, S. Kaxiras, A. Ros, A. Jimborean, and M. Själander, “**Understanding Selective Delay as a Method for Efficient Secure Speculative Execution**”, *IEEE Transactions on Computers (IEEE TC)*, vol. 69, no. 11, pp. 1584-1595, Aug. 2020.

N. Reissmann, J. C. Meyer, H. Bahmann, and M. Själander, “**RVSDG: An Intermediate Representation for Optimizing Compilers**”, *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 19, no. 6, Dec. 2020.

C. Sakalis, A. Jimborean, S. Kaxiras, and M. Själander, “**Evaluating the Potential Applications of Quaternary Logic for Approximate Computing**”, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 16, no. 1, Oct. 2019.

Y. Umuroglu, C. Davide, L. Rasnayake, T. B. Preusser, and M. Själander, “**Optimizing Bit-Serial Matrix Multiplication for Reconfigurable Computing**”, *ACM Transactions on Reconfigurable Technology and Systems (TRETSS)*, vol. 12, no. 3, pp. 1-24, Aug. 2019.

K.-A. Tran, T. Carlson, K. Koukos, M. Själander, V. Spiliopoulos, S. Kaxiras, and A. Jimborean, “**Static Instruction Scheduling for High Performance on Limited Hardware**”, *IEEE Transactions on Computers (IEEE TC)*, vol. 67, no. 4, pp. 513-527, Nov. 2017, **Paper of the month, April 2018**.

T. Carlson, K.-A. Tran, A. Jimborean, K. Koukos, M. Själander, and S. Kaxiras, “**Transcending Hardware Limits with Software Out-of-order Processing**”, *IEEE Computer Architecture Letters (CAL)*, vol. 16, no. 2, pp. 162-165, Feb. 2017, **Best of CAL award 2017**.

A. Bardizbanyan, M. Själander, D. Whalley, and P. Larsson-Edefors, “**Designing a Practical Data Filter Cache to Improve Both Energy Efficiency and Performance**”, *ACM Transactions on Architecture and Code Optimization (TACO)*, vol. 10, no. 4, pp. 54:1–54:25, Dec. 2013.

P. Gavin, D. Whalley, and M. Själander, “**Reducing Instruction Fetch Energy in Multi-Issue Processors**”, *ACM Transactions on Architecture and Code Optimization (TACO)*, vol. 10, no. 4, pp. 64:1–64:24, Dec. 2013.

T. Hoang-Thanh, M. Själander, and P. Larsson-Edefors, “**High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit**”, *IEEE Transactions on Circuits and Systems, I: Regular papers, Invited for SOCC Special Issue (TCAS-I)*, vol. 57, no. 12, pp. 3073-3081, Dec. 2010.

M. Thuresson, M. Själander, M. Björk, L. Svensson, P. Larsson-Edefors, and P. Stenström, “**FlexCore: Utilizing Exposed Datapath Control for Efficient Computing**”, *Journal of Signal Processing Systems*, vol. 57, no. 1, pp. 5-19, Oct. 2009.

M. Själander, and P. Larsson-Edefors, “**Multiplication Acceleration through Twin Precision**”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, vol. 17, no. 9, pp. 1233-1246, Sep. 2009.

- M. Islam, M. Själander, and P. Stenström, “**Early Detection and Bypassing of Trivial Operations to Improve Energy Efficiency of Processors**”, *Microprocessors and Microsystems: Embedded Hardware Design*, vol. 32, no. 4, pp. 183-196, Nov. 2008.
- PEER-REVIEWED CONFERENCES K.-A. Tran, C. Sakalis, M. Själander, A. Ros, S.Kaxiras, and A. Jimborean, “**Clearing the Shadows: Recovering Lost Performance for Invisible Speculative Execution through HW/SW Co-Design**”, *Proceedings of the ACM International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 241-254, Oct. 2020.
- R. Nishtala, V. Petrucci, P. M. Carpenter, and M. Själander, “**Twig: Multi-Agent Task Management for Colocated Latency-Critical Cloud Services**”, *Proceedings of the ACM International Conference on High-Performance Computer Architecture (HPCA)*, Feb. 2020.
- C. Sakalis, S.Kaxiras, A. Ros, A. Jimborean, and M. Själander, “**Efficient Invisible Speculative Execution through Selective Delay and Value Prediction**”, *Proceedings of the ACM/IEEE International Symposium on Computer Architecture (ISCA)*, June 2019.
- C. Sakalis, M. Alipour, A. Ros, A. Jimborean, S. Kaxiras, and M. Själander, “**Ghost loads: what is the cost of invisible speculation?**”, *Proceedings of the ACM International Conference on Computing Frontiers (CF)*, pp. 153-163, May 2019.
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