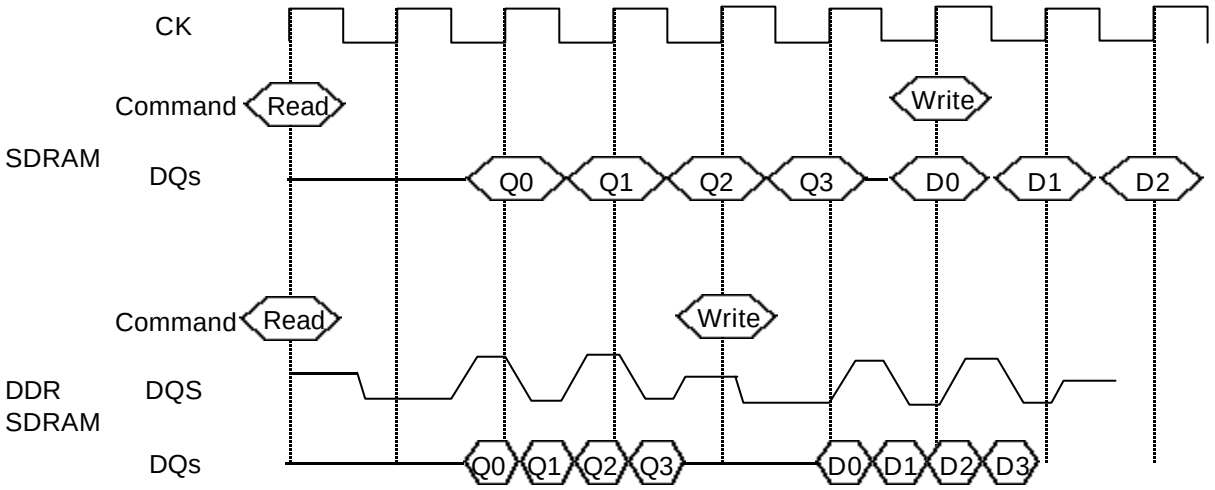
Key points for controller design

(1) General concept of DDR SDRAM

DDR SDRAM stands for “Double Data Rate Synchronous DRAM”. The term “double data rate” can be used for any product using both edges - high and low going- of periodically transitioning signal from “1” to “0” (or vice versa), for example clock or data strobe.
DDR SDRAM uses bi-directional Data strobe(DQS) moving with DQs in parallel so that receivers of DDR SDRAM and memory controller can use DQS as a reference signal to fetch corresponding DQs. One DQS may reply for 4 or 8bits of DQs. Fundamental benefit of using DQS is to realize high data transfer rate per pin through reducing access time of SDRAM and the propagation delay between DRAM and memory controller. Except them, we can also ignore the skew between the input clocks of DRAM and memory controller. All the above are possible with DDR SDRAM because DQS and DQs move in parallel. Figure 1 shows the general concept of DDR SDRAM. To help understanding, comparison timing to SDRAM is also shown.

< Figure 1: Basic concept of DDR SDRAM >



Data Strobe(DQS) faces up the exactly same environment as Data(DQs) when there is any data transfer between DDR SDRAM and memory controller. Ideally, DQS and DQs have the same physical characteristics like Cout on package and trace length on a board so that even though there are any environment changes such as, temperature and Vcc, the effect will apply for both, DQS and DQ. That means that there is no additional skew between DQS and DQ during a data transfer from DDR SDRAM to controller or from controller to DDR SDRAM. Therefore we can realize very high frequency operation on a real system using DDR SDRAM. This document is including the analysis of frequency limitation with current DDR SDRAM and a brief idea to overcome the barrier.

(2) Comparison between DDR and SDR SDRAM

The idea of DDR SDRAM is very simple. DDR SDRAM has additional Data Strobe(DQS) pin on current SDRAM. However, because of DDR operation, there are couples of function changes from current SDRAM. Table 1 shows the comparison.

< Table 1: Comparison between DDR and SDR SDRAM >

Features		DDR SDRAM	SDRAM
General	Package	66pin TSOP-II	54pin TSOP II
	Organization	x4, x8, x16	x4, x8, x16
	Internal banks	4	2, 4
Performance	Applied clock	66Mhz ~	~ 143Mhz
	R/W data rate/pin	133Mbps ~	~ 143Mbps
	CAS latency	1.5,2, 2.5	2, 3
	Write latency	1	0
	Burst length	2, 4, 8	2,4,8,full page
Interface	I/O levels	SSTL	LVTTL
		option:LVTTL for Cmd	
Features	On-chip DLL	Yes	No
	Data Strobe(DQS)	Yes	No
	DQM Mask	Write only	Read/Write
	Data alignment	Edged on reads	Cented on reads
		Centered on writes	Centered on writes
	Power Down	Yes	Yes
	Clock suspend	No	Yes
	Burst read single bit write	No	Yes
	Auto precharge/precharge all	Yes	Yes
	Auto Refresh/Self refresh	Yes	Yes

Package is changed from 54pin to 66pin TSOP II. Interface is changed from LVTTL to SSTL_2. This interface change is mainly to support higher data transfer rate. However, if there is any requirement for LVTTL on command signals, it is also supported in different part number. For the detailed product features, please refer to the attached DDR SDRAM specification. Samsung's first generation of 64M DDR SDRAM is targeted to support 133Mhz input clock and 266Mhz data transfer rate. DDR SDRAM does not support full page burst, clock suspend and burst read single bit write which were supported in SDR SDRAM. For the detailed key new ideas, please refer to the following pages.

(3) Key AC specifications

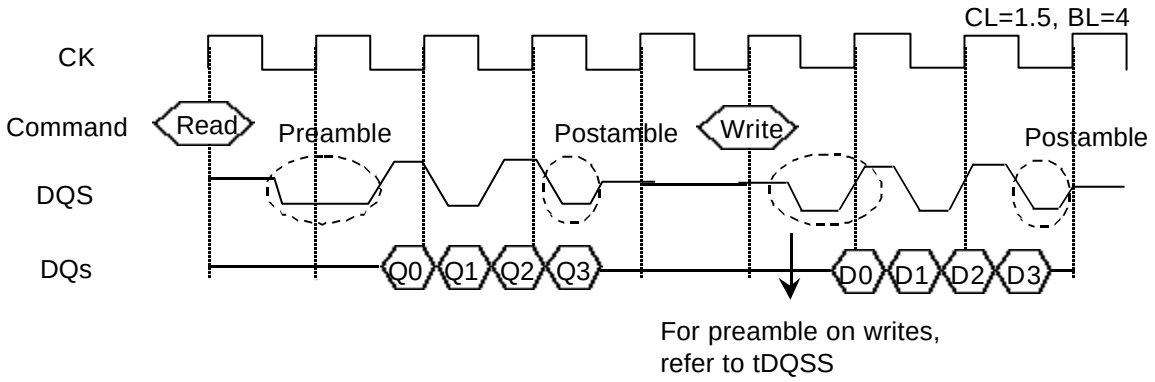
As we see in the previous chapters, DDR SDRAM is similar to SDRAM. However, we need to be careful to design a memory controller because of using DQS. SDRAMs use clock input for the reference signal to fetch data. DDR SDRAMs use DQS instead of clock. Therefore key changes from SDRAM are related to DQS. Through this chapter, key new features such as, pre- and postamble of DQS, tDQSS - the relationship between DQS input and data input into DDR SDRAM on write cycles, edge aligned data out and center aligned data in, new AC parameters , are presented.

1) Preamble and Postamble of DQS on reads

A. Specifications

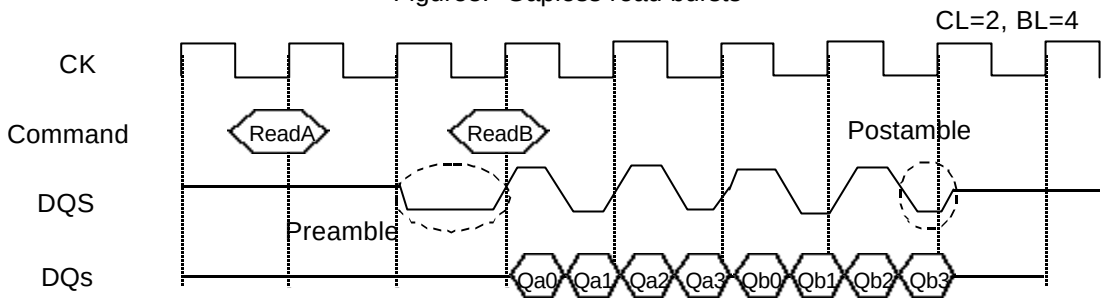
DDR SDRAM uses a data strobe signal(s),DQS, to increase performance. The DQS signal is bi-directional which toggles when there is any data transfer from DDR SDRAM to memory controller or from memory controller to DDR SDRAM.
Prior to a burst of read data, DQS signal transitions from Hi-Z to a valid logic low. This is referred to as the data strobe preamble. This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data (refer to figure 2).
Once the burst of read operation is concluded and given that no subsequent burst read operation, the output data strobe signal transitions from a valid logic low to Hi-Z. This is referred to as the data strobe postamble. This transition from logic low to Hi-Z nominally happens one half of clock period after the last edge of valid data (refer to figure 2)

< Figure2: data strobe preamble and postamble >



Consecutive or gapless burst read operations are possible from the same DDR SDRAM with no requirement for a data strobe preamble or postamble in between these operations. The output data strobe preamble is required before the device first drives the DQ pins (I.e., a DQ transition from Hi-Z to valid logic low). The output data strobe postamble is required when the device stops driving the DQ pins at the end of termination of burst (I.e., a DQ transition from valid data to Hi-Z). Figure 3 illustrates two consecutive or gapless burst operations from the same device and the required preamble and postambles.

< Figure3: Gapless read bursts >

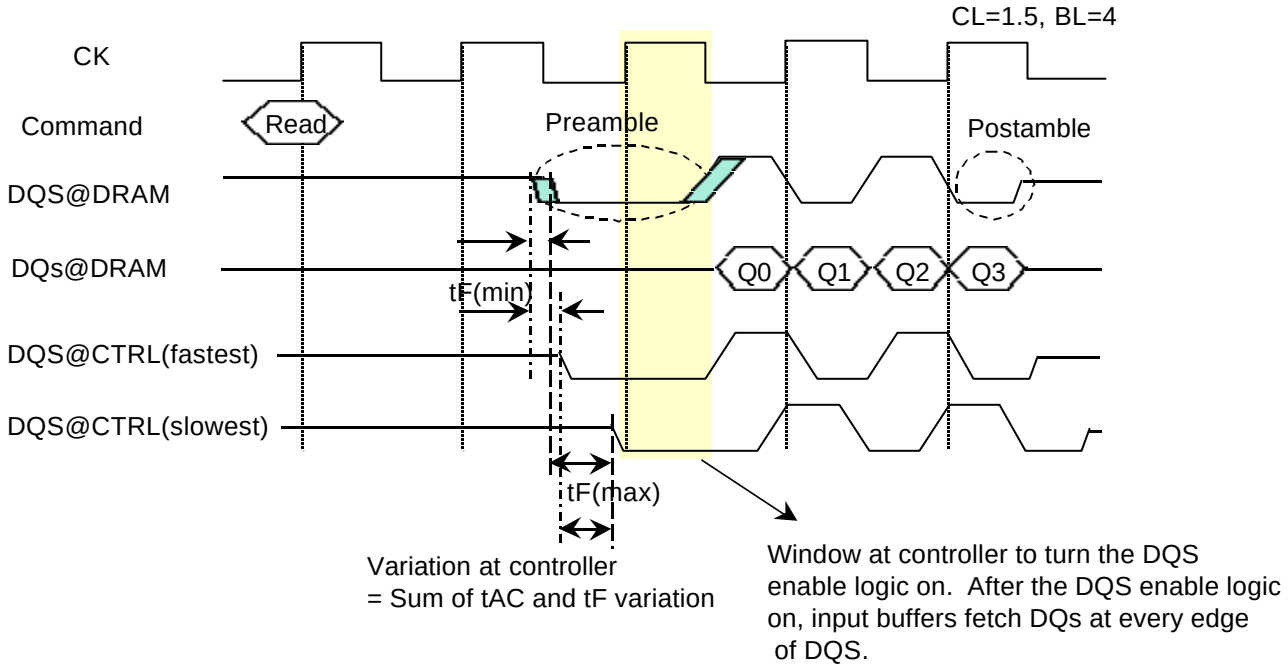


B. Receiver design point at controller

"Turn the input buffer(or DQS enable logic) of controller on during the preamble"

When there is no data transfer on DQ lines, DQS doesn't toggle and DQS pins keep Hi-Z. Since DQ and DQS use SSTL interface, the DQ and DQS lines are terminated on board. Therefore DQSs are charged with Vtt when there is no data transfer. (Vref is typically 0.45*Vcc for SSTL_3 and 0.5*Vcc for SSTL_2. Vtt level is same as V_{REF}. For the detailed SSTL interface information, refer to "EIA/JSD8-9.Sep. 1998".) Input receivers don't know what level it is, that is, Vtt can be logic high or low. If there is any noise on DQS lines, it may has the same effect as real DQS transition. Based on the above, when controller turns the DQS enable logic on, a stable logic level on DQS is required. To guarantee the stable logic status before any real data transition, DDR SDRAM defines preamble.

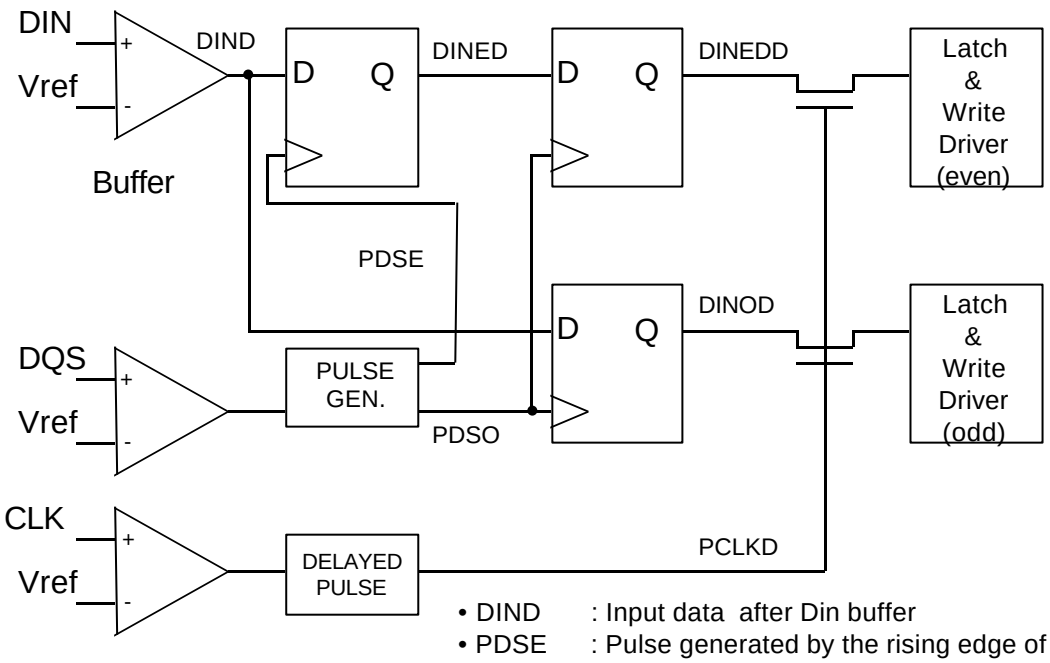
< Figure 4: Preamble and postamble at controller on memory reads >



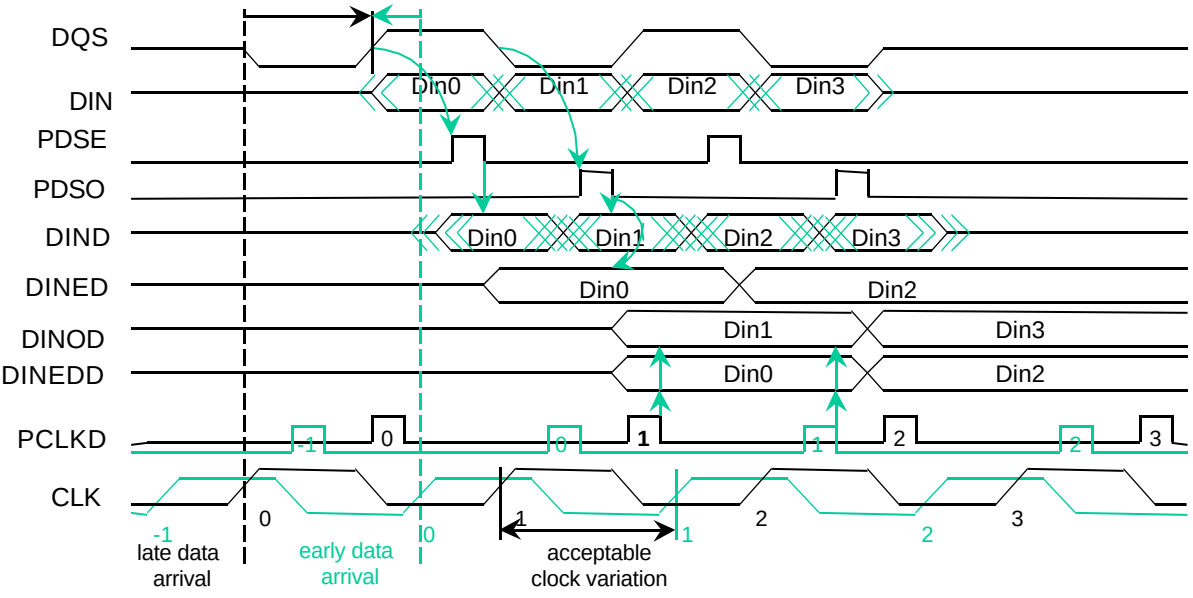
When there is no more subsequent data transfer after a burst read cycle, DQS transitions from logic low to Hi-Z. That means controller is required to turn the DQS logic off to avoid any kind of problem.

There is another way to control receiver input buffer. Instead of turning DQS enable logic on during preamble, postamble can be used to turn DQS logic off not to receive any more data after finishing a burst of read operation. DQS enable logic can be turned on any time before the first arriving data from DDR SDRAM. Even though invalid data are latched several times at the first step latch, they are not forwarded to the next step because enable signal of 2nd step latch is internal clock in this idea. For more detailed idea, refer to figure 5.

< Figure 5: an idea to control input buffer >

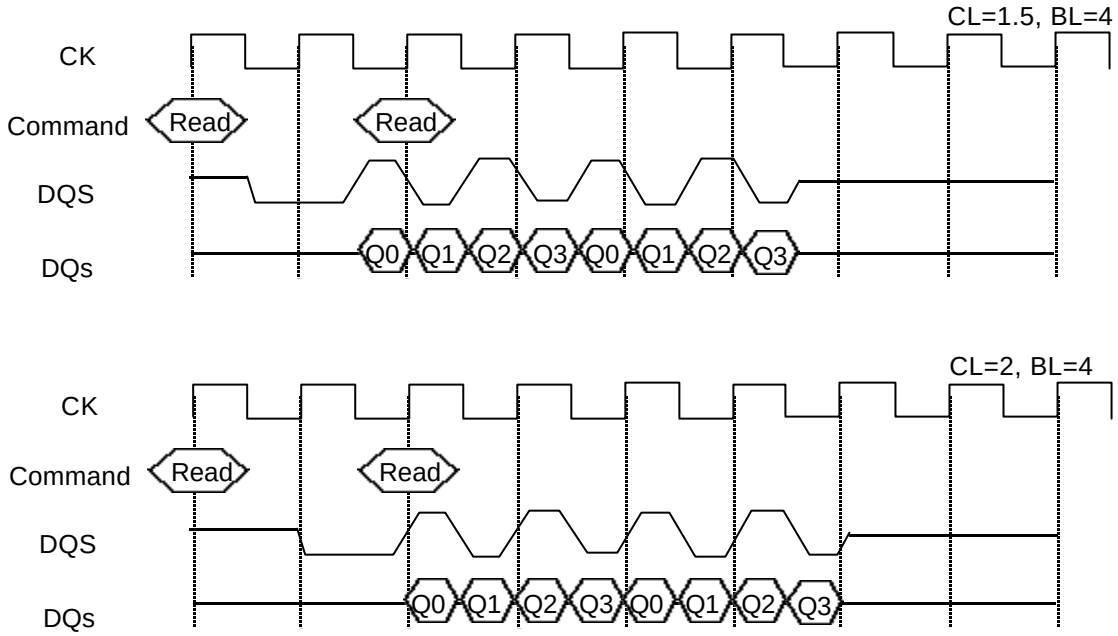


- DIND : Input data after Din buffer
- PDSE : Pulse generated by the rising edge of DS
- PDSO : Pulse generated by the falling edge of DS
- PCLKD : Internal Pulse generated by the rising edge of CLK

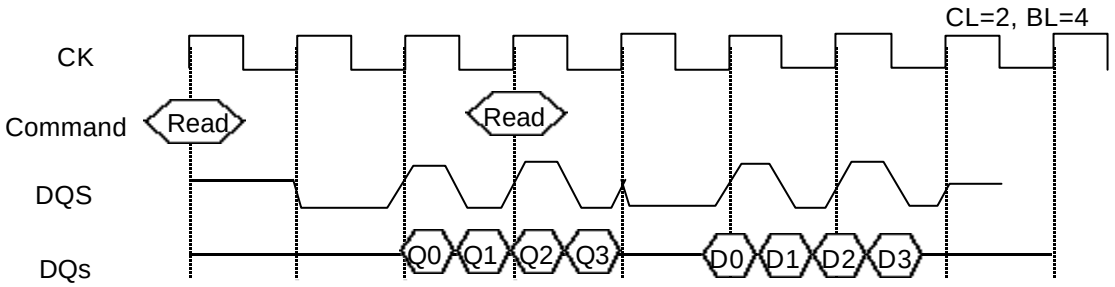


Memory controller designers need to pay attention related to preamble and postamble when they design a DDR SDRAM controller. In this chapter, combinations of consecutive commands are presented.

< Figure 6A : Read-Read timing diagram to one row >



< Figure 6B : Read-Read timing diagram to different rows >



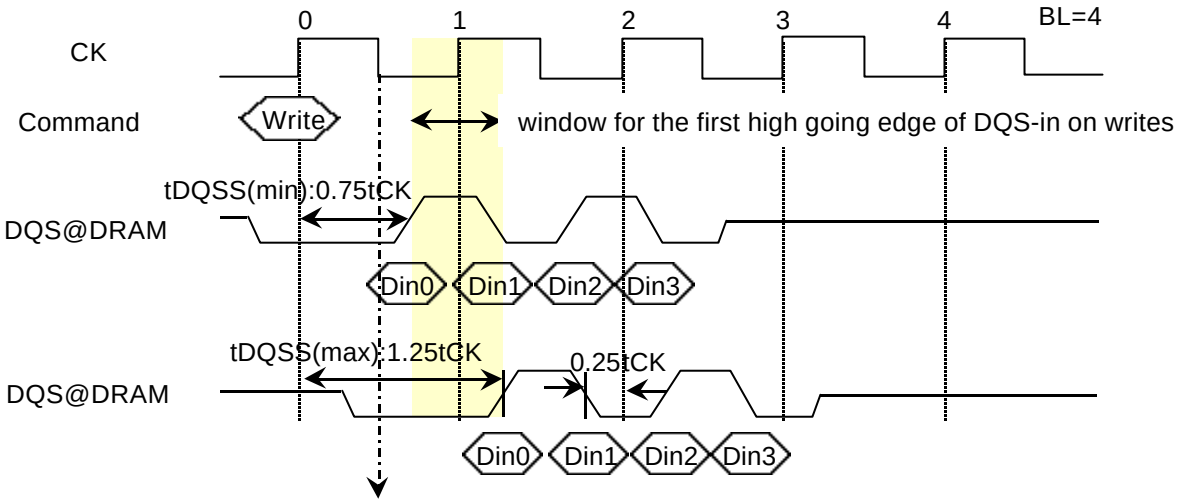
Row means external bank, not SDRAM internal bank. In case of consecutive memory access to different rows, DQSs come out from different device. Therefore, to avoid conflict between those two DQSs, one clock period of gap between the last DQS output of first read and the first DQS output of next read is required. However, if the consecutive reads are to one row, gapless read operation is possible because DQSs and DQs come out from one device. Figure 6A shows consecutive read accesses to one row and such as figure 6B to different rows.

2) tDQSS on writes

A. tDQSS specifications

DDR SDRAM defines tDQSS to turn the DQS enable logic on at right time and to guarantee a safe write operation in DDR SDRAM. DDR SDRAM turns DQS enable logic on after receiving write command. To get the DQS enable logic turned on, DDR SDRAM requires certain period of time. That is tDQSS(min). After receiving input data through input buffer, internal write operations occur. Even though we realize very high external data transfer rate using DDR(double data rate), internal operations, read and write, in DDR SDRAM can not meet that high speed. To solve the problem, the internal data bus width of current DDR SDRAM targeting 266Mbps is twice the external data bus. That means internal operation in DDR SDRAM starts after receiving two subsequent input data. The second data has to be received at input buffer 0.25tCK before the second clock edge from write command for internal write operation. Write latency at DDR SDRAM is conceptually one. The term “conceptually one” means there is no write latency relative to DQS, but almost one clock latency relative to input clock,CK. That affects the write recovery time.

< Figure 5: tDQSS- Write command to the first DQS rising edge delay >

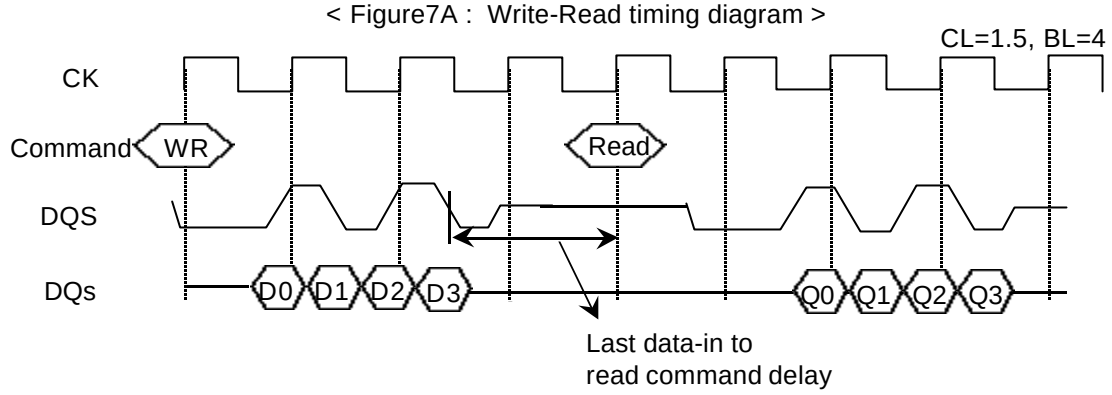


At this point, DQS has to be valid logic low.
That means there is no limitation of preamble cycle time as long as DQS keeps valid logic low at the next falling edge of write command in.

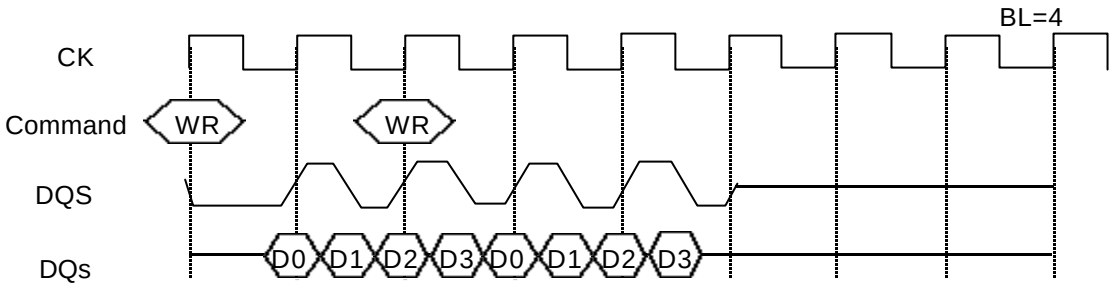
B. Controller design point to meet tDQSS

Controller designers need to consider the DQS output delay at controller and flight time from controller to DDR SDRAM. The first high going edge of DQS-in has to be arrived in the range of tDQSS. In addition, when there is a write followed by read cycle, read command can be issued one and a half clock after the last data-in because of the write recovery time. Figure 7 shows write-read timing diagram.

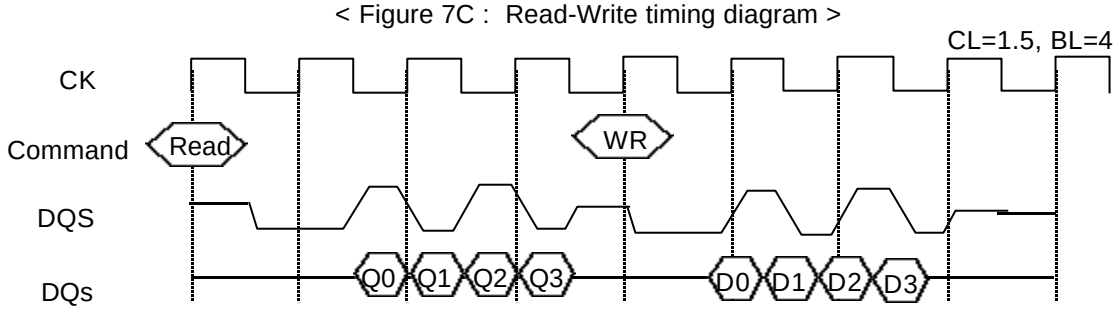
< Figure7A : Write-Read timing diagram >

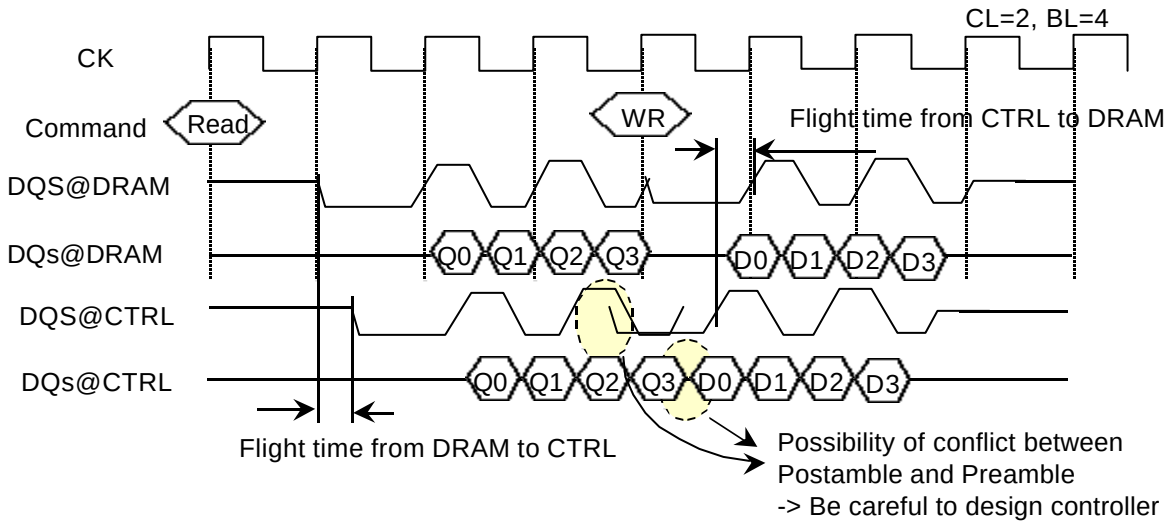


< Figure 7B : Write -Write timing diagram >



< Figure 7C : Read-Write timing diagram >



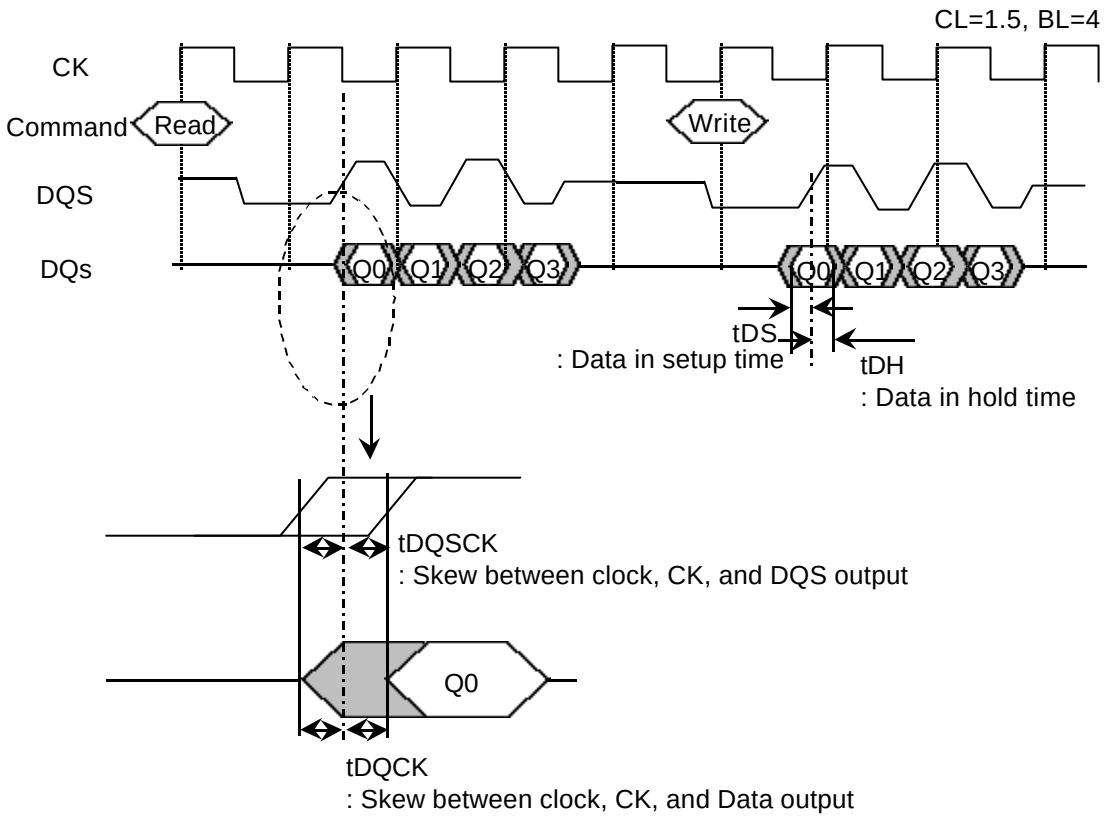


3) Edge aligned read and Center aligned write

A. specification

The relationship between DQS and DQ is “Edge aligned on reads, Center aligned on writes”
Edge aligned on reads means that the edges of DQ outputs are coincident with the edges of DQSs.
Center aligned on writes means that the edges of DQSs are placed at the center of valid input data window.
Because of edge aligned read, ideally there has to be no skew between DQS and DQ. However, in reality, there will be small skew called tDQSQ.

< Figure 8: Basic read and write operation >



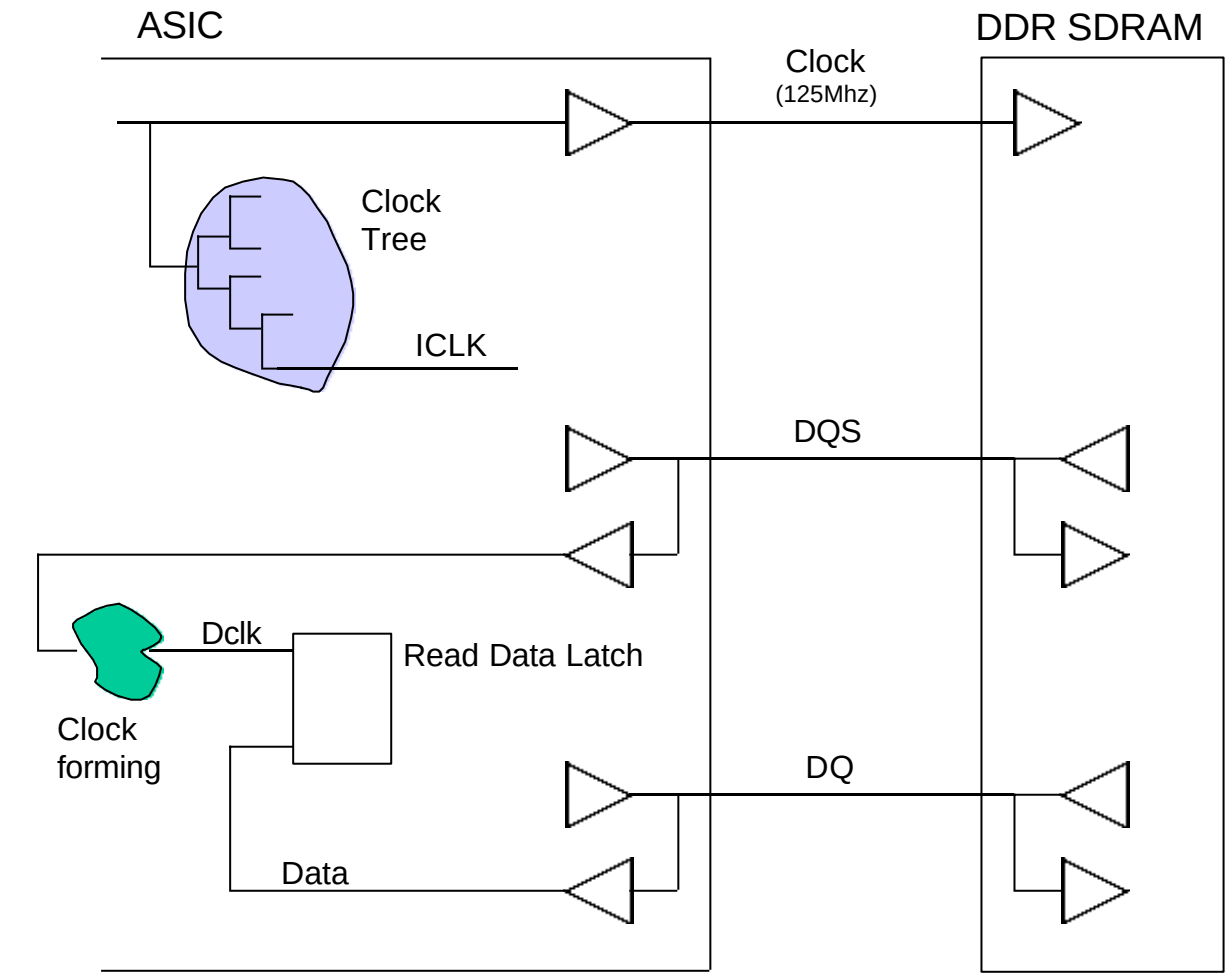
B. Controller design point

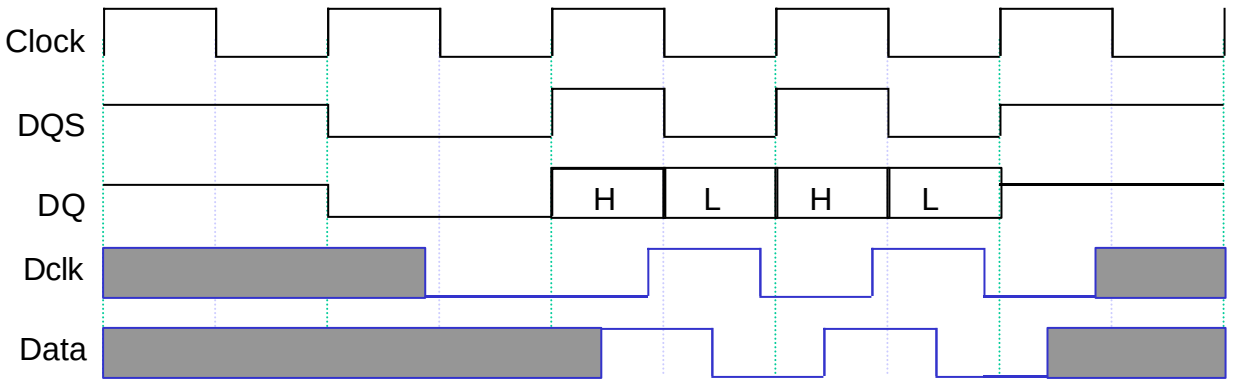
Receiver circuit at controller needs to make certain amount of delay on DQSs to fetch DQs at DQS edges. If DQSs are shifted by 90 degree, DQ setup and hold time relative to DQS at controller internal circuit will be same. However setup and hold time at controller can be decided by receiver designers. Edge aligned read gives flexibility for setup and hold time to receiver designers. If they want different values for setup and hold time of their receiver, they can do it.

C. Example of DDR SDRAM interface

The following schematic shows a example of the logic within the controller macro which is inside the ASIC and how it connects to the DDR SDRAM The main area of concern is making Dclk from DQS. There are several kinds of methods to make 90-degree shifted clocks.

< Figure 9: DDR SDRAM Interface >

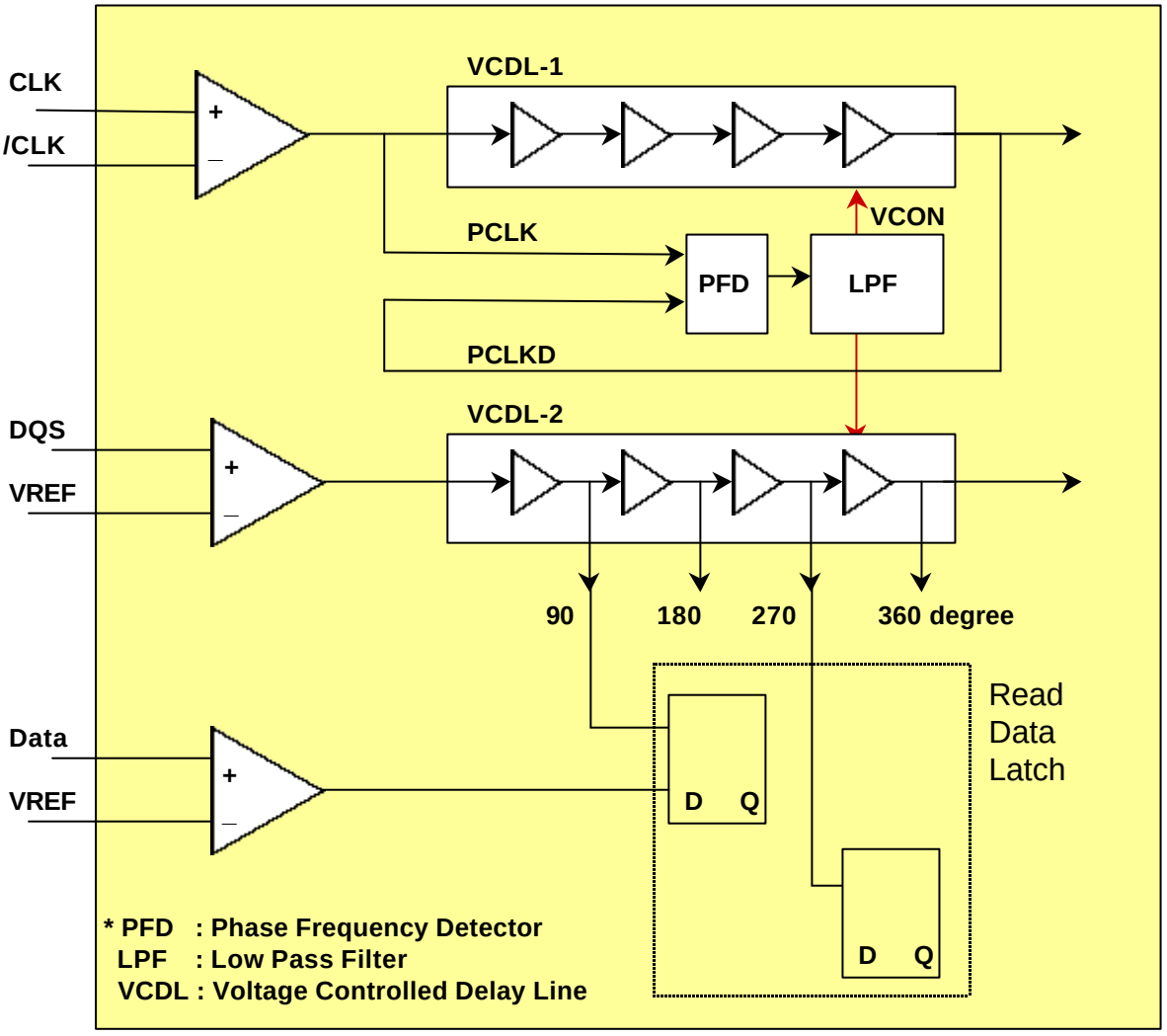




4) How to Make 90-degree shifted clock

A. Using DLL (Delay Locked Loop)

< Figure 10: Receiver scheme with DLL >

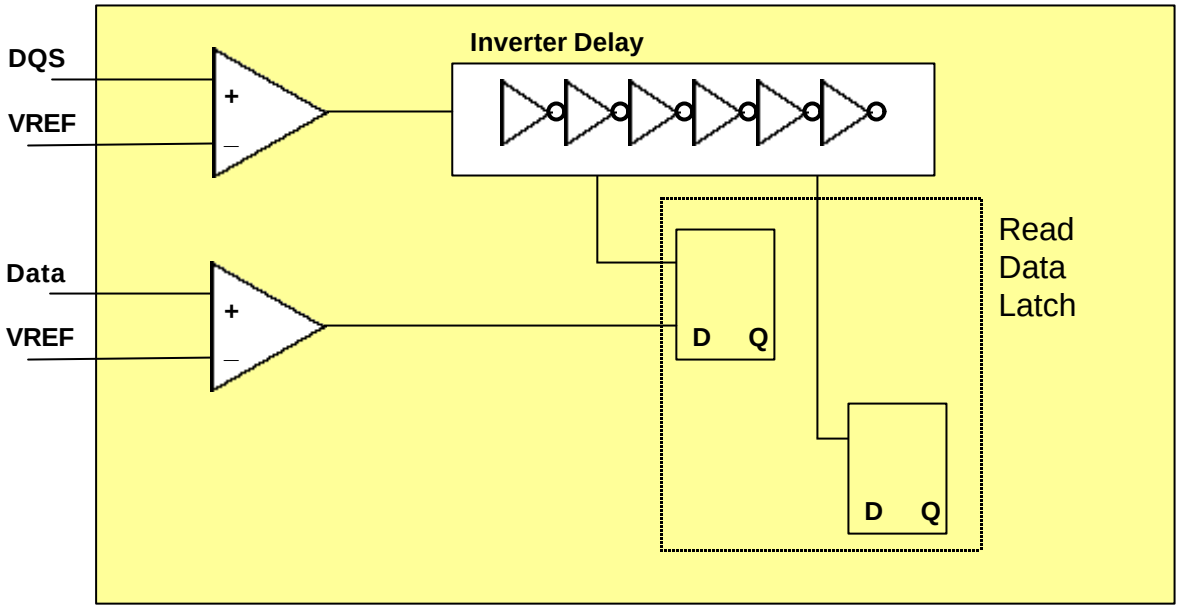


Using DLL is the popular way to make 90-degree shifted clock. Figure 10 shows the block diagram of the conventional DLL circuit. DLL is composed of Phase Frequency Detector(PFD), Low Pass Filter(LPF) and Voltage-controlled Delay Line(VCDL). After power-up PFD compares PCLK and PCLKD. If the rising edge of PCLKD is earlier than that of PCLK, LPF makes VCON low in order to increase the delay of VCDL-1(*1). If the rising edge of PCLKD is later than that of PCLK, LPF makes VCON up in order to shorten the delay of VCDL-1. Finally the rising edge of PCLK and that of PCLKD are synchronized. VCDL-2 is the copy of VCDL-1 and delay of VCDL-2 can be divided by 4. Therefore 90-degree shifted clock and 270-degree shifted clock can be made regardless of the clock frequency. In the case of burst length of 4, the first and third data should be fetched by 90-degree shifted clock and the second and forth data should be fetched by 270-degree shifted clock.

*1 : The delay of VCDL-1 can be increased when VCON is low: depends on circuit design.

B. Using inverter delay

< Figure 11: Receiver scheme with inverter delay >



Using inverter delay is the simplest way to center the DQS in the middle of the data window but it is hard to make fixed delay which is the independent of the PVT(Process Voltage Temperature) variation. We recommend using voltage temperature independent circuits such as internal voltage regulator with Band Gap Reference(BGR).

C. For your reference

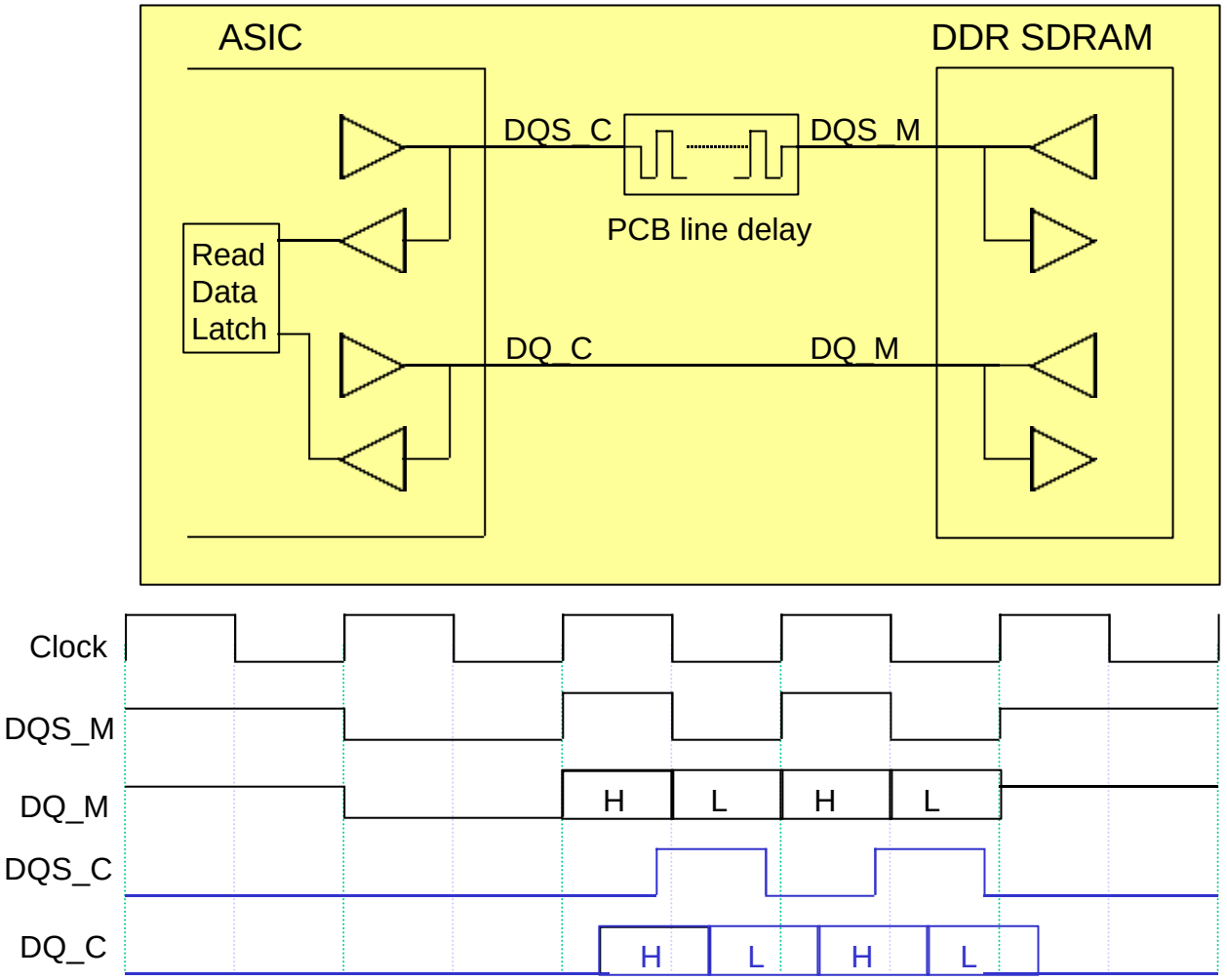
There are many kinds of timing control methods such as analog Delay Locked Loop(DLL), Digital DLL , Synchronous Delay Line and Synchronous Mirror Delay.

Here is references for you.

1) I.A. Young, J.K. Greason, J.E. Smith and K.L. Wong, " A PLL clock generator with 5 to 110MHz lock range for microprocessors," ISSCC Digest of Technical Papers, PP.50-51, Feb. 1992
2) J.G. Maneatis and M.A. Horowitz, " Precise delay generation using coupled oscillators," ISSCC Digest of Technical Papers, PP.118-119, Feb. 1993
3) C. Kim, J. Lee…."A 64MB/s Bi-directional Data Strobed, Double-Data-Rate SDRAM with 40mW DLL Circuit for a 256MB Memory System," ISSCC Digest of Technical Papers, PP.158-159, Feb. 1998
4) Saeki, T., et. Al.," A 2.5ns Clock Access 250MHz 256Mb SDRAM with a Synchronous Mirror Delay," ISSCC Digest of Technical Papers, PP.374-375, Feb.1996 and IEEE J.Solid-State Circuits, vol.31, no.11, pp.1656-1668 Nov. 1996
6) Okajima,Y.,et. Al.," Digital Delay Locked Loop and Design Technique for High-speed Synchronous Interface," IEICE Trans. Electron./ vol. E79C, no.6, pp. 1136-1144, Nov,. 1993
7) Hatakeyama, A., et. Al., " A 256Mb SDRAM Using a Register-Controlled Digital DLL." ISSCC Digest of Technical Papers, PP.72-73, Feb.1997
8) Dunning, J., et. Al.," An All-Digital Phase-locked Loop with 50-Cycle Lock Time Suitable for High Performance Microprocessor," IEEE J.Solid-State Circuits, vol.30, no.4, pp.412-422, Apr. 1995

D. Using PCB line delay

< Figure 12: Receiving scheme with PCB line delay >



Using PCB delay line is the simplest and robust way to center the DQS in the middle of the data window. In the case of 125MHz Operation, adding delay line of 2ns between DQS_C and DQS_M is needed in order to get the same amount of setup and hold time. Our characterization said that to get 2ns delay needs 11 inch PCB delay line. However it is not always necessary for all controllers to make the edge of DQS in the center of DQ. The minimum delay of PCB delay line is the sum of DQ-to-DQS skew(tDQSQ) and controller's setup time. Assume the setup time of controller is 0.3ns and tDQSQ is 0.5ns, 4~5 inch delay line is enough to make setup time of 0.3ns .