Tutorial: Characterizing SDRAMS

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Abstract

This paper presents characterization methods for an SDRAM in a manufacturing environment. Contact tests, dc tests, basic functional tests, signal margin tests and retention characterization are shown. Measurement of the cell signal is used as an example for pico probing. Special test modes for SDRAMs which can be used to aid characterization and failure analysis (FA) are discussed.

1. Introduction

DRAMs, and now SDRAMs, are one of the primary products used for driving higher integration densities. It is a commodity product, so it can be fabricated in large volumes. Large volumes are needed to establish uniformity in a given fabrication process. Process problems result in failing memory cells. These fails can be easily located due to the regularity of the memory array. The SDRAM combines logic for decoding with analog circuitry for sensing the cell signal. Logic and analog performance of the device can be measured. Development of a new product needs verification of the design, analysis of yield and circuit problems and characterization of the SDRAM.

Verification checks all specified parameters against the data sheet of a product. Fails are sorted out and analyzed. The analysis focuses on means to find the root cause of a given problem. This results in process or design changes. Characterization deals with the behavior of the device under different operation conditions. These operating conditions can well be out of the specified range. It helps general understanding of the functionality and performance limitations of a device. Since characterization is not focussed on a special problem compared to analysis, it has a lower priority in a production environment.

Characterization consists of all methods to measure the functional performance of a product under different operation conditions. Some of these results are used to improve the fabrication process, some help to understand the function of the circuit to generate a functional model, others are used to improve test coverage and to enhance the quality of shippable product. This tutorial deals with characterization. The starting point of characterization is in most cases the analysis of a given problem. Characterization doesn't stop after identifying the root cause, but looks at all influencing parameters and how they affect performance.

This tutorial starts with an overview of a general production flow of a new SDRAM design. It shows typical test gates to verify functionality and yield definitions. A block diagram of an SDRAM is used to explain the functionality. A timing diagram is used to show basic operation and important timing parameters.

First, according to a normal test flow dc measurements are presented followed by the analysis of basic screen fails with bit fail maps of a chip, a wafer or a lot. The next section deals with test strategies for signal margin tests and timing tests. Pico probing for internal cell signal measurement is also shown. Correlation with indirect methods can be achieved. Characterization with Shmoos will be explained. Special test modes enabling further characterization are discussed.

2. Manufacturing Flow

Figure 1 shows a typical test flow for an SDRAM. There are 5 electrical test gates. Every gate operates at different temperatures and voltages. This gives the first two important parameters for characterization: Temperature

Prefuse Test	HT 2.7V/3.9V Ycont, Ydc,Ys,Ys1,Yts
Fusing	
Postfuse Test	HT 2.8V/3.8V Ycont, Ydc,Ys,Ys1,Yts
Assembly	
Burn-In	120C 5.0V Yts
Cold Temperature Test	LT 2.9V/3.7V Yc,Ydc,Yts
Hot Temperature Test	HT 2.9V/3.7V Yc,Ydc,Yts

Figure1: A typical SDRAM manufacturing Testflow

and voltage.
These parameters are specified in a DRAM data sheet:

Absolute Maximum Ratings
Operating temperature range .....0 to + 70 C
Storage temperature range.....– 55 to + 150 C
Input/output voltage..... – 0.3 to Vdd+0.3 V
Power supply voltage VDD / VDDQ..... – 0.3 to + 4.6 V
Power Dissipation.....1 W
Recommended Operating Conditions unless otherwise noted
T A = 0 to 70 o C, Vdd = 3.3V +-0.3V

Yields are also visible in Figure 1**.** They are defined as the number of good chips divided by the number of total chips tested. Contact Yield (Ycont) looks for gross fails on the chip. Missing pads, shorts or opens directly at the inputs. This also measures the performance of the test equipment. Poor contact at the needles or dirt in the fixtures can affect contact yield.
A dc yield (Ydc) measures the current at different operating conditions.
A screen yield (Ys) measures the basic functionality of a chip such that every memory cell is written and read or can be repaired. SDRAM memory processes have implemented redundant memory cells to replace defect cells. A basic read-write test is called a screen test. Cells failing to a basic read-write operation are called hard fails. Perfect yield (Ys1) is determined as the number of chips which have no hard fails divided by the total number of chips.
There is also the test sequence yield (Yts). This can be given as absolute yield compared to the total number of chips on the wafer or as relative yield compared to the number of screen test good chips. The test sequence consists of retention time tests, some signal margin tests and some speed tests. The retention test checks for cell leakage between two accesses. The signal margin test writes a low signal into the cell and checks for correct function. These tests are modified for characterization. DC tests give analog value readouts, which are monitored. Additional test for internal voltage monitoring can be implemented. Fail counts are measured and analyzed to see process variation.

3. SDRAM Functionality

In order to characterize SDRAMs properly, knowledge of the internal circuits and their function during operation is needed. An SDRAM data sheet shows a block diagram (Figure 2).
Control logic and a timing generator select an operation mode. The basic operation mode of an SDRAM can be configured for a CAS latency and burst length. During any access, a row address (x) and a column address (y) are used to select a memory location. A bank select signal, which is supplied with the row and column address,

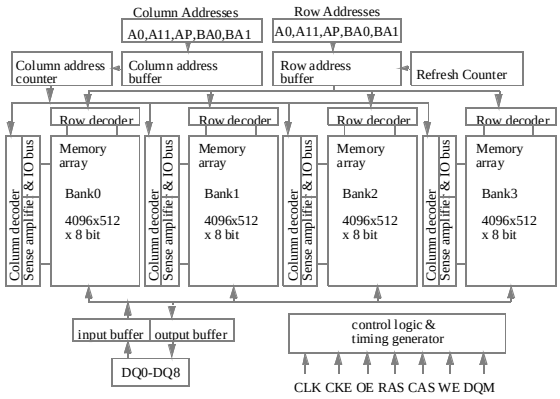

Figure 2: A block diagram of an SDRAM

selects one of four banks. The information is either read from the memory location or written through the data path. Input and output buffers connect the data to the external pins.
For every row address, a word line (WL) is selected and all cells along the word line are read out to sense amplifiers and refreshed with a write back. A column select connects one sense amplifier to the data path. Information is transported to the outside during a read. A write transfers data from the external pads to the sense amplifiers and can flip the sense amplifier to the opposite data.
SDRAM commands, addresses and data are latched at the rising edge of a clock (CLK). Basic SDRAM operation consists of an activate (ACT), read (RD) or write (WR) operation followed by a precharge. Additional commands (NOP, DESL) are used as time fillers. A refresh command (REFR) refreshes all cells for one row address in all banks.
A typical access is shown in Figure 3. The CAS latency of

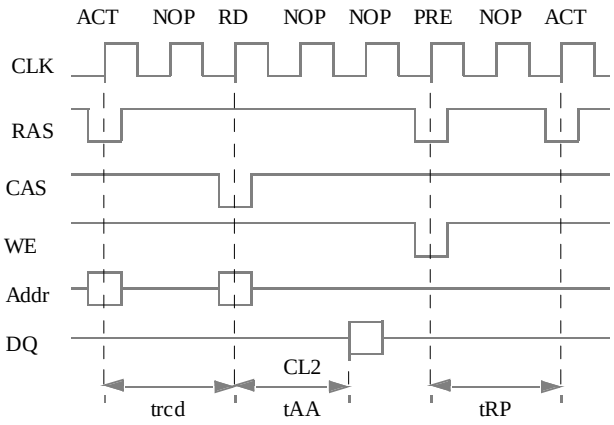

Figure 3: Timing diagram of an access of an

2 can be seen since the data is available at the outputs 2 cycles after the read. Since only one data bit is coming out, a burst length of 1 is selected. The latency is necessary to give enough time for internal operation from column address selection to valid data at the outputs. Important timing parameters due to internal operation are trcd, taa,trp,tww.

Trcd (typically 20ns) is the time between the activate command and the first read or write command. Internally a WL has to be decoded and the cell has to be read out to the sense amplifier before a column select can connect the sense amplifier to the data lines. Taa (typically 20ns) is the time needed to select a column and transport data from the sense amplifier to the output pads. Trp (typically 20ns) is the time where the cell is disconnected from the sense amplifiers and the sense amplifiers are equalized to be ready for the next access. Tww (typically 20ns) is the time needed to transport data from the inputs over the data lines to the sense amplifiers, which are decoded with the right column address, and over the bit lines into the memory cell.

4. Contact check

Contact check is a basic form of DC characterization. A current is applied to a needle and a voltage is measured. Since all the pads have input protection diodes a forward bias can be measured. Typically, a current of 100uA is used for forcing. Due to contact conditions, measurements give values between 500 and 800mV. The exact value depends on the temperature and the size of the diode. Open contacts will lead to –2V if the power supply has a compliance of 2V. A short in the input structure will give 0V as a reading. Characterization deals with looking at the complete trace V(I) and the temperature dependence of the curve (Figure 4 and Figure 5).

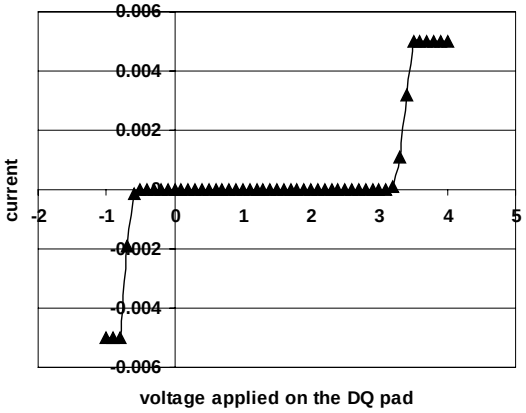

Figure 4: V(I) curve of an input diode

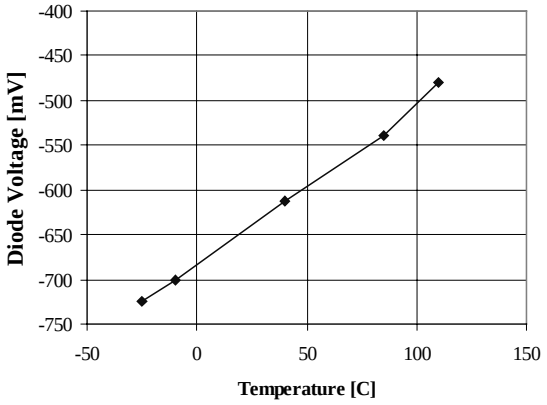

Figure 5: Temperature dependence of a diode voltage

5. DC Characterization: standby and active current measurement

From the data sheet (Table 1), other important DC values such as: standby current (ICC2), active current (ICC1) and no operation current (ICC3).can be seen. Large defects will cause a dramatic increase in the standby current. For standby current measurements a voltage is applied to the chip and the chip is initialized but not

Table 1: DC specifications of an 64Mbit DRAM

Operating Currents (T_A=0 to 70 C, Vdd = 3.3V 0.3V)
(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		**Symb.**	**-7**	**-7.5**	
			max.		
OPERATING CURRENT		ICC1			
trc-trcmin, tck=tckmin					
Outputs open, Burst Length =4, CL=3		x4	120	110	mA
All banks operated in random access,		x8	130	120	mA
all banks operated in ping-pong manner		x16	150	140	mA
to maximize gapless data access					
PRECHARGE STANDBY CURRENT in Power Down Mode	tck=min	ICC2P	2	2	mA
$\overline{CS}$=VH(min), CKE<=Vil(Max)	tck=infinty	ICC2PS	1	1	mA
PRECHARGE STANDBY CURRENT in Non-Power Down Mode	tck=min	ICC2N	45	40	mA
$\overline{CS}$=VH(min), CKE>=Vil(Max)	tck=infinty	ICC2NS	5	5	mA
NO OPERATING CURRENT	CKE>-VIH(min.)	ICC3N	55	50	mA
tck = min, $\overline{CS}$ = VIH(min)					
active state (max. 4 banks)	CKE<=VIL(max.)	ICC3P	8	8	mA

active.

Gross defects can be measured by using a so called ‘hot spot’ method. Liquid crystal is applied on top of the chip. Polarized light is used. With different temperatures, the refractive index of the liquid crystal changes. Shorts cause high currents, which in turn heat up the chip. In the defective region the liquid crystal heats up (gets dark) and a ‘hot spot’ can be seen (Figure 6). To find it easily, a voltage pulse can be applied. The dark spot, where the fail

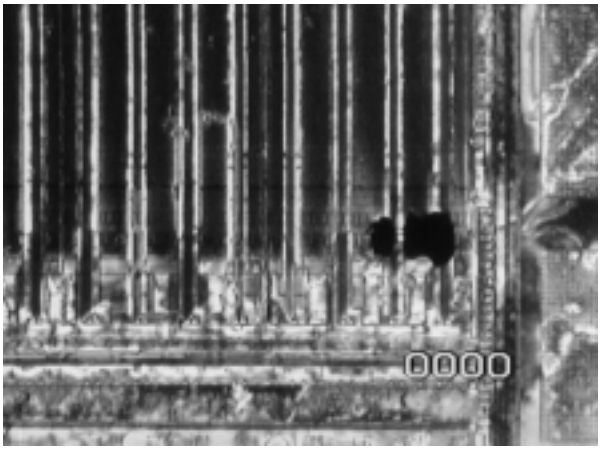

Figure 6: 'Hot spot" of a short in a driver

occurs, pulses according to the external voltage pulse. Distributed shorts and internal voltage regulators make the analysis much more difficult.

A typical SDRAM has a voltage for the logic periphery called an internal regulated voltage (Vint=2.5V) and an array voltage slightly lower (Vblh=2.0V). Vblh determines the level of the signal in the cells. Since all cells along a WL are activated at the same time up to 16k sense amplifiers are set at once. To lower power consumption, the array voltage is low. To write the full level of 2.0V into the cell, a boosted WL voltage (Vpp=3.7V) is needed. Vpp has to be at least one threshold voltage above the array voltage.

To limit the leakage current of the cell underneath the array transistor, a back bias voltage (Vbb=-1V) is applied for the n-channel devices. Since half array voltage sensing can be used, another voltage Vblh/2 has to be generated. Characterization can break down the current in different components for the different voltage networks and different operations. [1] shows the data dependence of the active current due to bit line coupling and the extraction of current components by varying internal voltages.

(Figure 7**:**) The I_{vbhl} variation with the supply voltage and the rest of the current can be calculated by putting a trend line into the graph with the equation:

I_{cbr} = 20.27 mA/V Vblh +0.67 mA

I_{vblh} (V_{blh}=2.0V)= $dI_{cbr}/dVblh$ * 2.0V = 40.7mA

The rest of the current is needed for periphery and WL voltage networks. I_{rest}= 0.67 mA

6. Basic screen test

A basic screen test consists of a voltage level applied to the chip, a pattern which determines the operation and a timing set. Van de Goor [2] has implemented a notation for specifying a test pattern and a fail type. A simple basic screen test uses a March test. Data is written to the whole

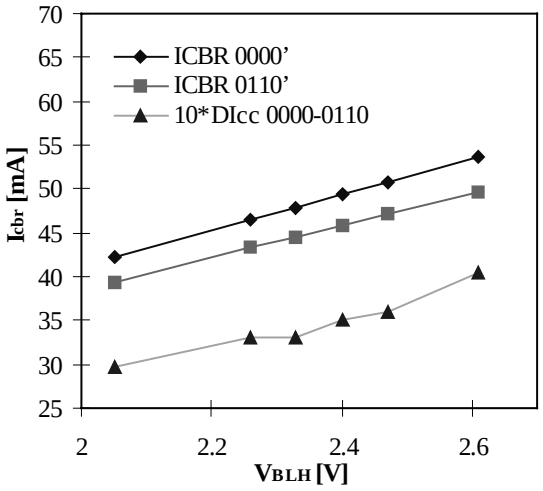

Figure 7: Current dependence on voltage and data topology

array followed by a read of the same data. Opposite data is written and then read through the entire array. A write of normal data concludes the pattern. Since 5 operations are performed on all N memory cells this is a March5N. This leads to the following notation:

{⇑(r0);⇑(r0,w1);⇑(r1,w0) }

This test covers stuck at faults and addressing faults. The arrows denote the counting sequence. An SDRAM needs a row (x) and a column (y) address. Therefore, the counting sequence can count for each y address all x addresses (x-fast) or count for every x address all y addresses (y-fast). Since all cells along one x address are refreshed in each access, there are no retention issues with a fast x pattern. This is the preferred pattern for characterization. For a fast y pattern, an asynchronous refresh has to be implemented to guarantee the specified retention time. Since all other faults have analog behavior in an SDRAM they will be tested with signal margin tests or retention tests. Fails can be stored in a catch ram, which represents the memory or a fail vector memory.

Figure 8 shows a typical chip bit map from a catch ram. Different fail categories are shown. Column select, WL, BL and single cell fails can be seen. The fail types can be distinguished by their appearance on the bit map. Fails can be associated with certain process levels. BLBL shorts, for example to a metal process. It is easy to feedback this information to the process owners if bitmaps are available. Therefore, wafer maps (Figure 9) and lot maps (Figure 10) are generated. Wafer maps can point out certain problem areas like the center or the edge of the wafer. Lot maps can show chamber dependencies if every second wafer shows a different picture. These maps are more valuable than a simple pass/fail information.

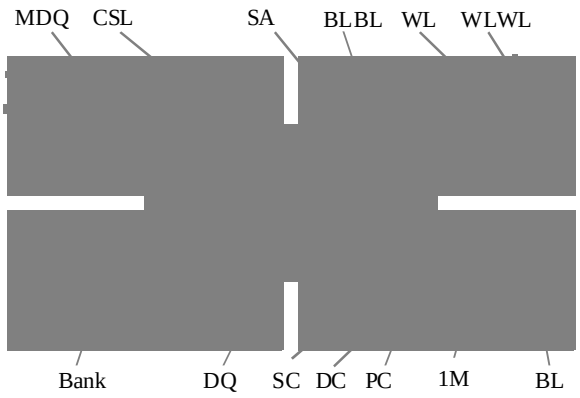

Figure 8: A typical chip bit map with fail signatures

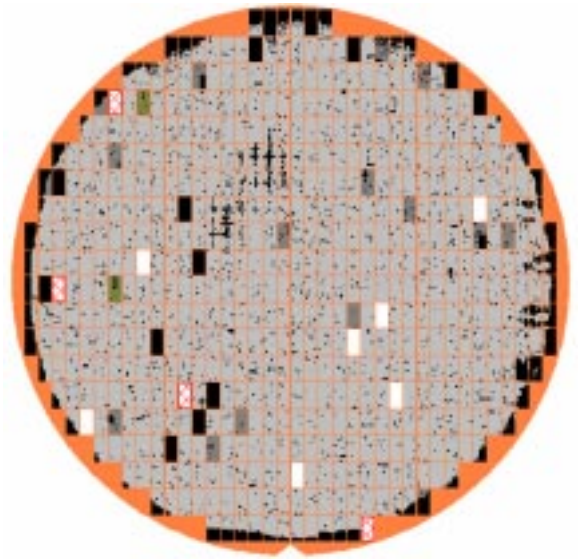

Figure 9: A wafer bit fail map

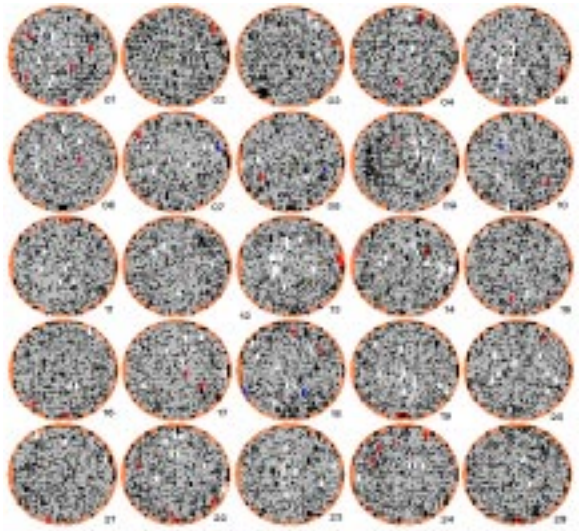

Figure 10: A lot bit fail map

Detailed information of the fail root cause can be extracted.

7. Test sequence

This section deals with signal margin tests and retention characterization. Signal margin tests check for the correct function of the cell with a reduced signal. To maintain leakage and readout conditions a bump test where the internal array voltage (Vblh) is bumped van be used. At low array voltage, 10-20% lower than normal (0.1/1.9 or 0.2/1.8V), the memory cells are written. Then the voltage is bumped back to normal conditions. Normal leakage will occur. Finally data from the cells is read out. Similarly the Vpp voltage can be lowered to limit the signal of a '1' (2.0V) to a value of Vpp-Vth. Figure 11 shows the dependence of fail counts on Vpp voltage. It is debatable whether or not a signal margin test should be combined with a retention test. For characterization, retention and signal margin tests should be separated to distinguish between fail signatures.

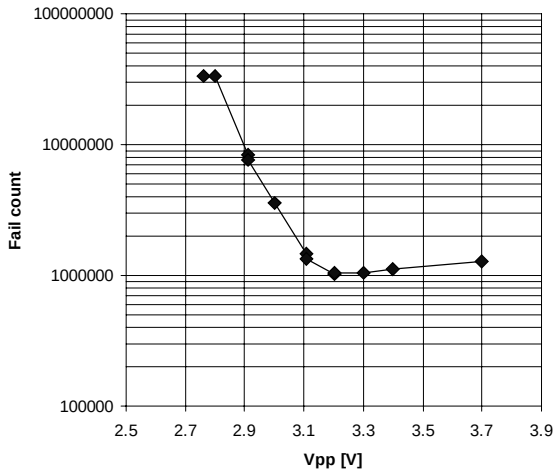

Figure 11: Fail count depending on Vpp

Retention tests count the number of fails at a given retention time (Figure 12). Since an SDRAM uses a capacitor as a storage element, the charge in the capacitor is lost over time due to leakage to the surroundings. The retention time is the time between two accesses of the same cell. This translates into the time between the access of the same WL. Accessing all WLs refreshes the whole memory array. A typical retention curve is pictured in Figure 12. The number of failing cells increases with retention time. There is an intrinsic retention time due to signal limitations and an extrinsic part of the curve, the tail of the curve at lower retention times, due to defects. Voltage and temperature dependencies are also understood. Higher temperature increases the fail count.

Higher voltage increases the number of fails in the tail due to gate induced drain leakage current (GIDL), but helps

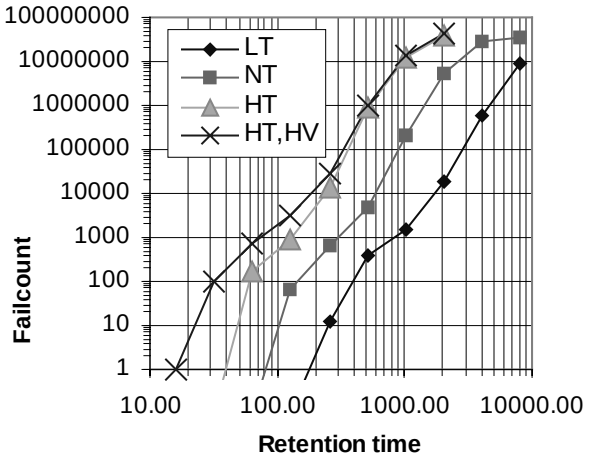

Figure 12: Temperature and voltage dependent retention fail count

the intrinsic fail count because of the larger cell signal. This characterization shows the dominant parameters: temperature and voltage. The understanding of the leakage mechanism can help optimization of the process.
Characterization can also deal with analysis at even or odd WLs. Misalignment can influence the retention time of the cells. Figure 13 shows a retention time dependent fail count of even and odd WLs. A small difference can be seen. This is still within tolerance of the alignment. These effects can help to improve fail analysis.

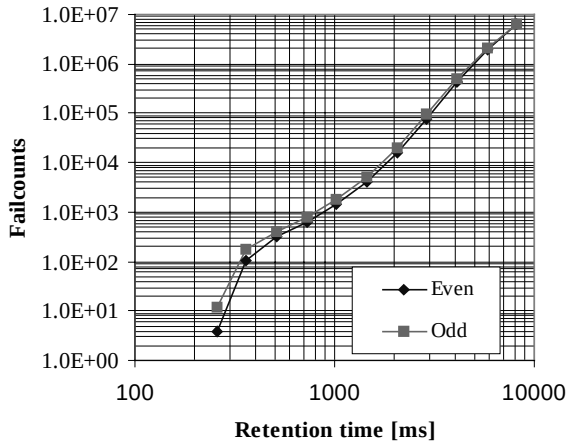

Figure 13: Effects of WL alignment on retention fail count

8. Speed testing and Shmoos

Speed testing verifies performance of the SDRAM according to specifications. SDRAMs operate at frequencies up to 133 MHz. Conventional memory testers operate at 25..75 MHz. To achieve higher frequencies, more than one pattern generator is operated in parallel. 2, 4 or 8 generators are used in parallel and multiplexed. Problems arise due to noise on the lines at high frequencies. Characterization normally uses slower test systems. To achieve testing for timing parameters fill cycles can be dropped and asynchronous timings can be used. For measurement of trcd, a simple timing diagram is

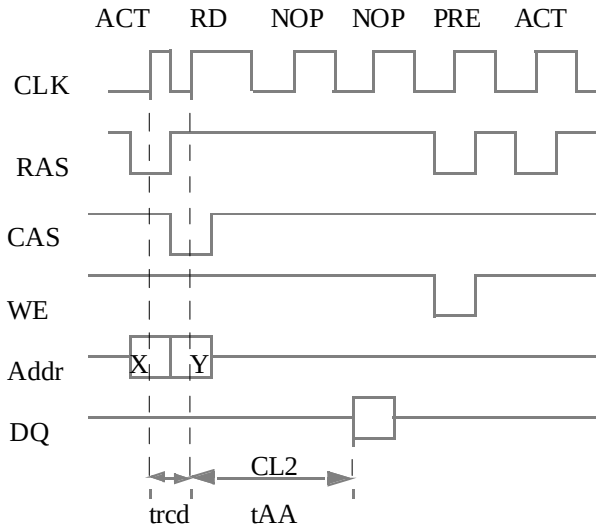

Figure 14: Timing diagram for a trcd

shown in Figure 14.
The NOP cycles between ACT, RD, PRE and ACT are dropped. Some cycles are needed for the CAS latency of 2. The clock signal in the ACT cycle comes late and the CLK signal in the RD cycle comes early. Limits for the timing variation are set by the minimum CLK rise and fall times and the cycle length. Looking for pass or fail information and varying one or two parameters is referred to as a Shmoo. Typically Vcc can be chosen as the second variable. Figure 15 shows a resulting Shmoo for a 64M SDRAM. The '*' region denotes a fail, the '-' a pass region. [3] shows an overview of the Shmoo technique. The Shmoo in Figure 15 indicates that the part is regulated. Above a certain voltage, trcd is fixed. At lower voltages trcd increases. The Shmoo with simple pass/fail information can be extended to show a fail count. At the pass/fail boundary, a bit fail map of a chip can be generated (Figure 16). The signal distribution for trp can easily be seen. Areas farthest away from the signal distribution fail first. This can help looking for the most time critical path on a chip.

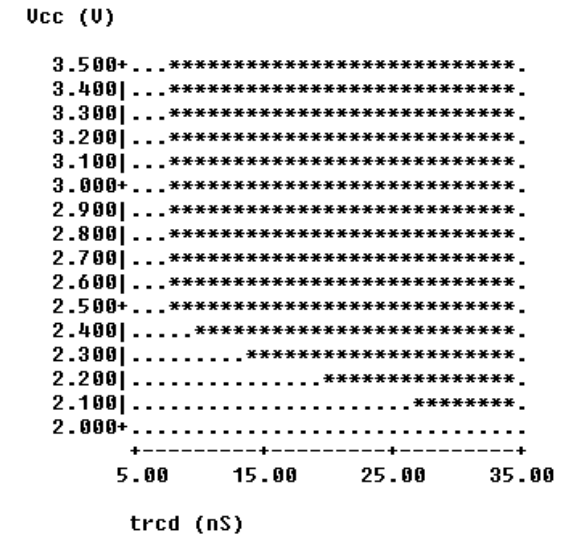

Figure 15: Shmoo plot of trcd and Vcc

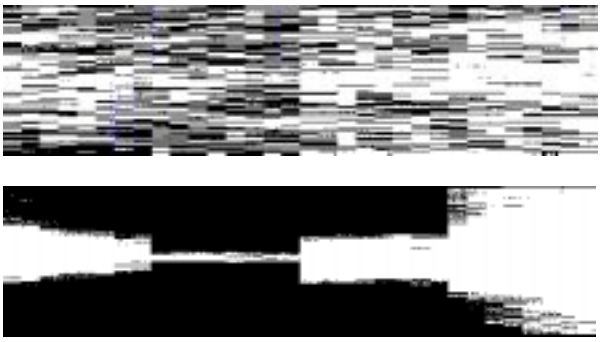

Figure 16: Bit fail map for a minimum trcd and trp

9. Pico probing

Pico probing is the measurement of internal signals during operation of the chip. A characterization tester is needed for supplying an endless repeated pattern. An oscilloscope samples the waveform during the repeating pattern. A synchronization pulse connects the scope to the tester to allow sampling of the signal. An active pico probe is a small needle attached to a MOS or bipolar transistor. The MOS transistor has the benefit of having a small input capacitance of less than 30fF to minimize loading of the measured circuit. A preamplifier is connected to the pico probe to generate the signal for the oscilloscope. In an advanced design, special test pads are incorporated to allow access to signals at the last metal layer. Figure 17 shows a typical measurement setup.

An example of pico probing is measurement of the cell signal and the sensing operation. Special test pads are available on some designs for true and complement bit line. Two 28C MOS Pico probes one connecting the true bit line, the other the complement bit line are used. The capacitance of the pico probe is low (<30fF), so that the sensing is not affected. The bit lines have around 200fF capacitance and the cell around 40fF. The time scale is 2 ns/div, 20ns total range. An endless pattern with a write data, write opposite data operation is applied to verify sensing and writing of 1 and 0. During the write the cell is sensed and then flipped to the applied data. Averaging of waveforms is necessary to get clear signals. Differential

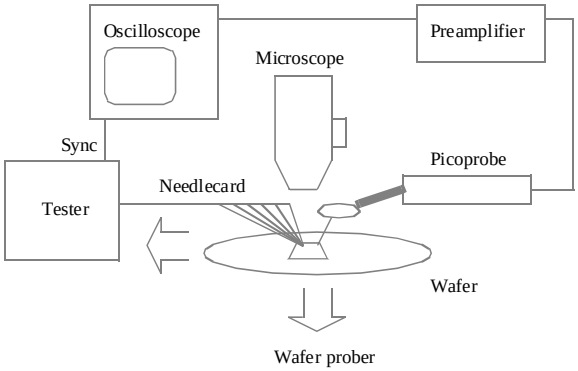

Figure17: Picoprobe measurement setup

measurement is used to suppress noise on the signal. The same Pico probe is used for measuring true BLs and complement BLs. Instead of moving the Pico probe from the true BL to the complement BL, it is possible to simply change the addressed WL moving from a cell at the true BL to a cell at the complement BL. The following effects are measured: the signal for a '1' and '0', BL coupling, SA coupling, WL coupling, Isolator and Equalizer coupling. Figure 18 shows the schematic of the sense amplifier.

Due to different patterns along a WL, the coupling of the adjacent bit line or sense amplifier affects the signal.

Table 2: Signal on the true BL depending on the data along the WL

WL	data	BL	SA	Signal	Value
2	0xF	-	-	-	'1'
1	0xF	up	up	Up	BL+SA 40mV
1	0x1	down	down	Up	Reference WL
1	0x0	down	up	up	SA 20mV
1	0x0	down	down	Down	Signal -20mV
2	0x0	-	-	-	'0'

Figure 19 shows the measured signal. A measurement without any signal on the bit line is used as reference. The signal for the '1' and '0' is 200mV. With the table above, the BL and SA coupling can be determined as 20mV each. The isolator and equalizer couple 60mVdown

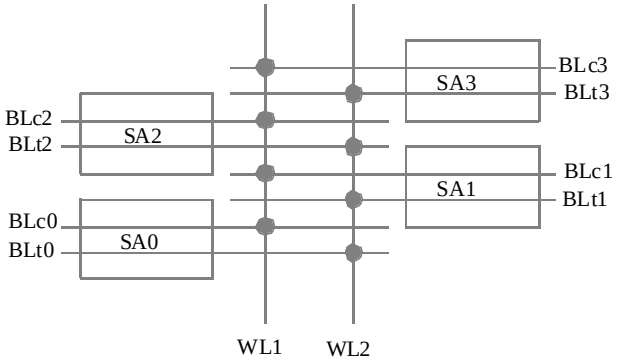

Figure 18: A schematic of the bit lines and sense amplifier

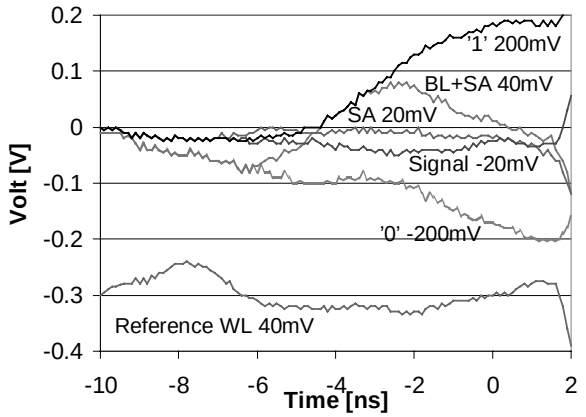

Figure 19: Pico probe signal measurement of the differential sense amplifier signal

before the WL comes up. The WL is coupling 40mV up on the selected bit line.

This measurement is a typical characterization effort. This gives understanding of the sensing scheme. It can help the designers to optimize the sense amplifier layout. No direct problem fix can be associated with this technique.

10. Testmodes

[4] presents test modes for a 256M DRAM. This is an example of what can be built into a design to facilitate characterization and analysis of a DRAM. Besides data compression modes which speed up test time, but don't help characterization, voltage trim options are the most helpful test modes. A test having a combination of high voltage for the periphery Vint, which gives operation speed and noise, and low voltage for the array Vblh, making a low signal in the cells, can give additional test coverage for the SDRAM product and help analyzing fails. Isolating a fail to be caused by a certain voltage condition on one of the networks helps in analysis. Changing of back bias or WL voltage helps retention characterization by determining the dominant leakage path for a given memory cell.

Special signal margin tests vary the voltage during write or the compare voltage during a read operation. The level actually stored in the cell can be changed. [5] gives an example of how to use a timing test mode and a voltage trim test mode to determine cell signal levels with a simple external test.

Timing options for changing the set delay, the time between WL up and sense amplifier enable, and the column select pulse are very useful. External timing control is limited by a clock latching all commands. Extra timing options help to compensate for this. All test modes allow more characterization even without pico probing or unpackaging a device.

11. Summary

This paper presents an overview of a typical SDRAM manufacturing test flow and associated characterization opportunities. Aspects of different test levels and their characterization are covered. Different characterization methods are discussed to study and understand the behavior of an SDRAM. Test strategies are shown to overcome test equipment speed limitations. Opportunities for the circuit designers to help characterization are mentioned. All of this shows the different aspects of characterization as an exciting field of developing new techniques to better understand the behavior of an SDRAM under different operation conditions. This knowledge is needed to speed up the analysis of problems. There are many fields left where characterization tools can be developed for bit map analysis, current analysis and shmoo techniques. New characterization methods are needed to analyze leakage current fails in a sub micron environment with many regulated voltage networks on one chip.

References

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