Dual Clock Scheme for over 200MHz Synchronous DRAM System

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Abstract

Dual clock scheme, where master clock (CLKM) and output clock (CLKO) are applied to a SDRAM with different phase, is proposed to achieve very fast access time without area / power penalty. A circuit technique to adjust the different phase between dual clocks is described. This scheme in conjunction with 2-bit prefetch architecture enhances operating clock frequency over 200MHz without PLL/DLL on chip. An experimental dual clock 16Mbit SDRAM demonstrates the clock access time of 2.5ns.

1. Introduction

A memory system using synchronous DRAMs (SDRAMs) requires very fast clock access time (tAC) to compensate transmission delay of signals on PCB, skew of inputs to SDRAMs and setup time to a memory controller. On the other hand, buffering of internal CLK in SDRAMs consumes 1 - 2ns, this causes slower tAC(4 - 5ns) than requirement. To cancel the buffering delay, DLL or PLL on chip were proposed. However, these circuits don't match SDRAM specifications because of its large power consumption (~100mA), long lock-in time(~1μs) and area penalty (>1%) [1]. This paper describes newly proposed dual clock scheme for very high speed tAC, and the circuit technique to implement it with 2-bit prefetch architecture.

2. 2-bit prefetch architecture

Maximum operating frequency of a SDRAM is limited by the longest pipeline stage, and usually it is from column address input to read data latch. To break this bottleneck, 2-bit prefetch architecture [2] is used as shown in figure 1. Column select lines (CSL) and pre-amplifier enable signals (PAE) for even / odd block are activated respectively, so that 2-bit data are transferred from sense amplifiers to double read latches concurrently. One read data is latched to the forward one, and the other data to the backward one, depending on the initial column address. Because 2 clock cycles can be assigned to this stage, it is no longer the bottleneck of the frequency. This architecture easily enables over 200MHz clock frequency operation.

3. Circuit design of dual clock scheme

Ext.CLKM is used for general purpose including input latching or counter triggering, while ext.CLKO is used for data output processing only. CLKO is always supplied earlier than CLKM with phase difference of 'tDIFF'. Timing chart of read operation is shown in figure 2A.

A READ command is asserted at the beginning of T1, and a pulse øread is generated to trigger a series of array control signals (CSL, PAE, etc.). After tRD, read data selected by CSL appear on the read buses for the even block (RDe) and the odd block (RDo) concurrently. RD select signal øe or øo is activated in the cycle T3, and either RDe or RDo is transmitted to RDs as shown in figure 2B. A simplified circuit diagram of the øe/øo generator is described in figure 2C. When øread becomes high, initial column address CA0 is provided to the counter, shifted by CLKM and goes to the master-slave shift register. At the rising edge of CLKM in the cycle T3, CA0 is transmitted to the final NAND gates. At the falling edge of CLKO in the cycle T3, øe is activated (in this case initial CA0 =0), and either øe or øo is activated alternately after that. RDs is valid in T3 and ready to go to the final stage. When CLKO becomes high, the final clocked inverter lets the data on RDs pass to the output buffer. As a result, valid Dout is available in the cycle T4, and tAC =2.5ns in case tDIFF=1.5ns. Figure 2D shows the output enable signal øOE generator. The Burst Length & CAS Latency counter determines the delay cycle and period of øOE in synchronization with CLKM. However the last flip-flop is triggered by CLKO, in order to synchronize the enable timing of øOE with read data at the output buffer.

By using these circuit design, read data is processed by different phase clocks of CLKM and CLKO without confliction, and very fast clock access time is obtained. Figure 3 shows simulated waveforms of this circuitry.

4. Allowable range of phase difference

As data output is triggered by CLKO, tAC and tOH are adjustable to fit to each system by changing the phase of ext.CLKO. Allowable range of phase difference is determined by (1) column address access time (tCAC) and (2) joint circuitry shown in figures 2C and 2D.

(1) tCAC: Maximum tDIFF should be decided so as to satisfy the following relationship

(CL-1) tC - tDIFF + tAC' ≥ tCAC

where tC=clock cycle time, tAC' =access time from ext.CLKO, CL=CAS Latency.

In case of tC=5ns, CL=4, tAC'=4ns, tCAC=17ns, **tDIFF≤ 2ns**

(2) Joint circuitry: tDIFF max is also limited so as to assure correct operation of the joint circuitry described in figure 2C, 2D. Valid pulse width of øe or øo is required ≥1.5ns to transmit RDe/ RDo to RDs. Considering the master-slave register in figure 2C, the valid width is enabled by the rising edge of CLKM and disabled by the rising edge of next CLKO, that is, tC - tDIFF. Consequently, **tC - tDIFF ≥1.5ns**. In case of tC=5ns, **tDIFF≤ 3.5ns**.

(3) Minimum **tDIFF= 0ns**. In this case, a dual clock SDRAM becomes equivalent to a conventional single clock SDRAM.

5. Experimental 16MSDRAM with dual clock

Figure 4 shows an microphotograph of the experimantal 16MbitSDRAM with dual clock scheme. It was fabricated with 0.4μm double metal CMOS process. As total load of CLKM and CLKO is equivalent to that of the conventional single clock SDRAM, its area penalty is just 0.08% and additional operating current is just 3mA due to one more input buffer for CLKO. SSTL_3 (Stub Series Terminated Logic) is used as I/O interface. Figure 5 shows measured output waveform of the SDRAM. tAC of 2.5ns is demonstrated with tDIFF = 1.5ns. Table 1 summarizes the characteristics of the SDRAM.

An example of practical use of the dual clock SDRAM is described in figure 6. A PLL on the memory module generates CLKM and CLKO with appropriate phase difference. Because clock adjustment is closed in the module, very fast access time is available without user's attention.

6. Conclusion

Proposed dual clock SDRAM offers the following benefits to memory systems. tAC is very fast and adjustable with ext.CLKO. Area penalty and additional supply current are negligible. It becomes fully compatible with a conventional SDRAM when ext.CLKO is tied with ext.CLKM externally. It allows flexible system design.

References

[1] M.Horowitz,et al.,"PLL Design for a 500MB/s Interface", ISSCC DIGEST OF TECHNICAL PAPERS, pp.160-161, Feb. 1993.

[2] Y. Kodama, et al., "A 150-MHz 4-Bank 64M-bit SDRAM with Address Incrementing Pipeline Scheme", 1994 Symp. on VLSI Circuits, Digest of Technical Papers, pp.81-82.

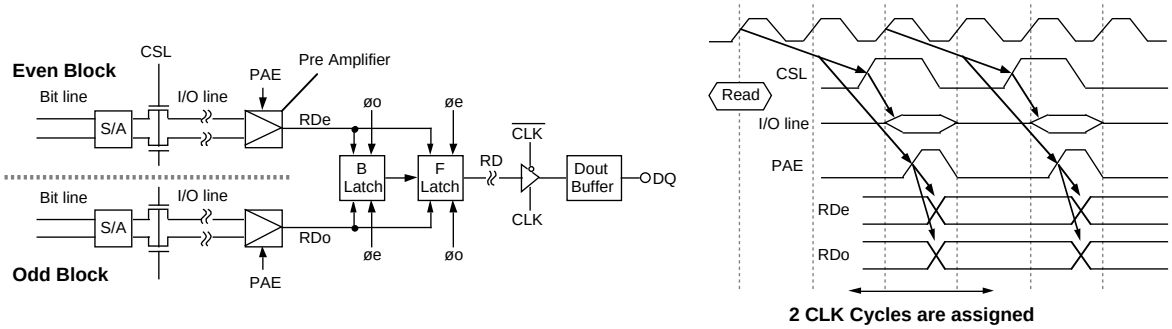

Fig.1 2-bit prefetch architecture

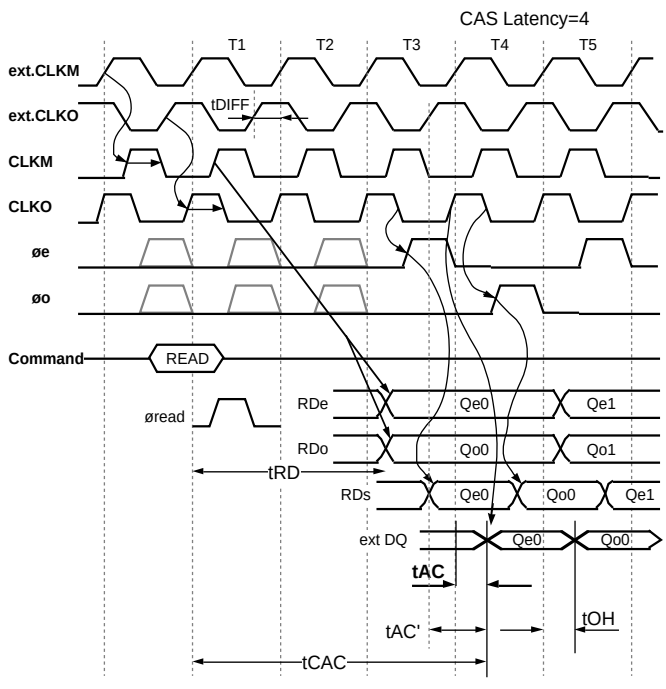

Fig.2A Timing chart of read operation

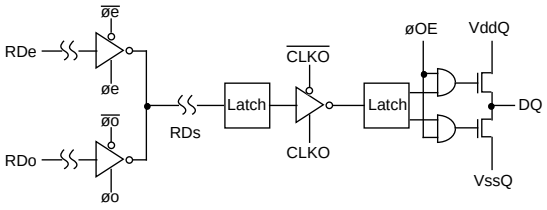

Fig.2B Read data path

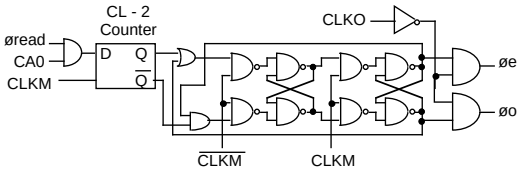

Fig.2C RD select signal generator

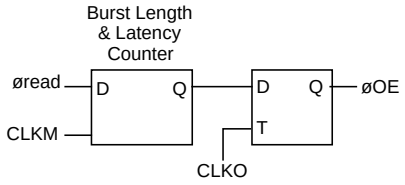

Fig.2D Output enable signal generator

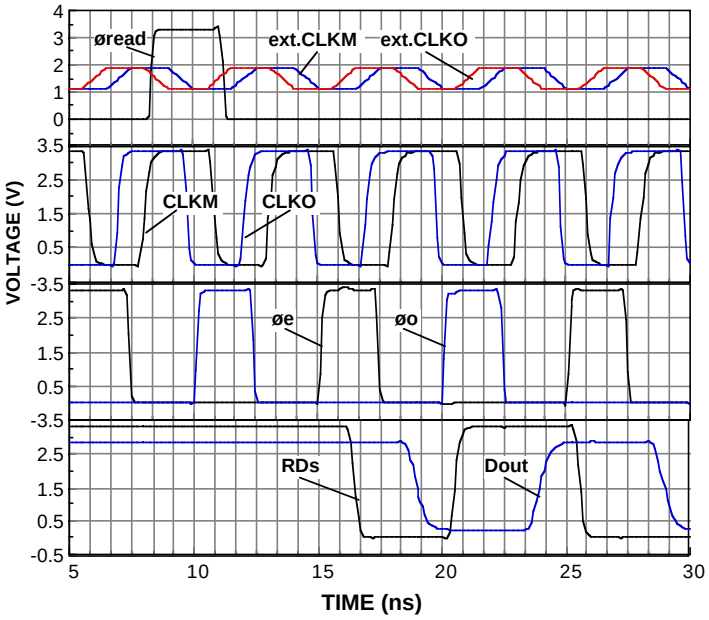

Fig.3 Simulated waveforms of dual clock scheme

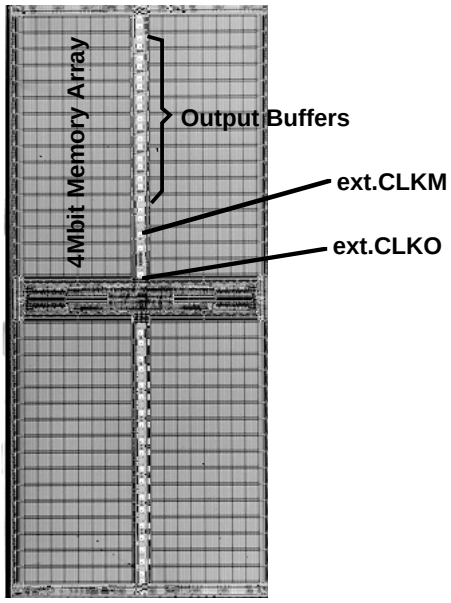

Fig.4 Microphotograph of the experimantal 16MSDRAM

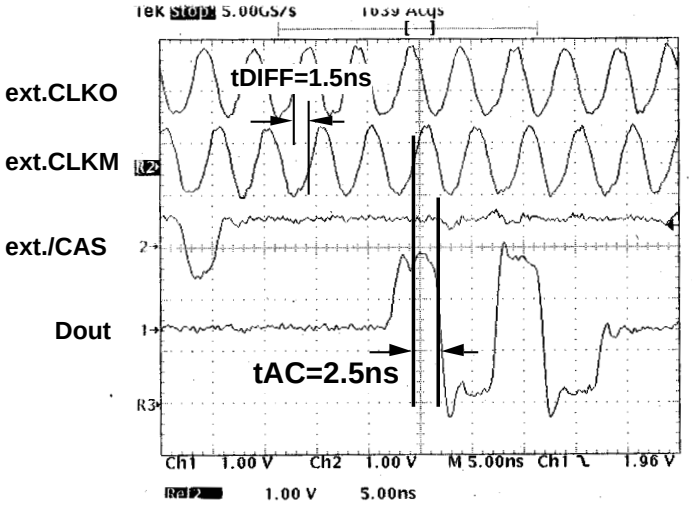

Fig.5 Measured output waveforms of the RAM

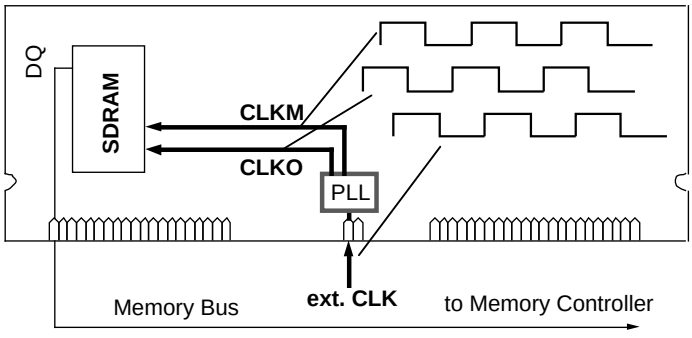

Fig.6 Example of the dual clock SDRAM module

Organization	4Mword x 4bit 2Mword x 8bit
Process Technology	0.4μm, CMOS double metal
Die size	70.0mm2
Cell size	2.24μm2
I/O Interface	SSTL_3
Access time (Vdd=3.3v, Ta = 25°C)	tCAC = 17ns tAC' =4ns tAC =2.5ns (tDIFF=1.5ns)
Supply current (Vdd=3.3v)	operating 120mA (tRC=70ns) stand-by 8mA
Number of banks	2
Burst length	1, 2, 4, 8
CAS latency	2, 3, 4
Burst type	sequential, interleave
Refresh cycle	4096 / 64ms
Package	400mil 44pin TSOP

Table 1 Summary of characteristics