LEON4: Fourth Generation of the LEON Processor

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Extended Abstract

The LEON4 SPARC V8 processor is designed to meet the increasing performance demands and low power requirements of current and future embedded and aerospace applications.

The LEON4 processor is an integral part of the GRLIB IP core library, which is a rich set of reusable IP cores, designed for System on Chip (SoC) development. The IP cores are centered around the common Advanced Microcontroller Bus Architecture (AMBA) on-chip bus, and are vendor independent, with support for different CAD tools and target technologies. A unique plug&play method is used to configure and connect the IP cores, which provides for rapid development of advanced SoC designs.

The advances made by the LEON4 processor, which are presented in this paper, makes the GRLIB IP core library suitable for designing high-performance and low-power SoC designs of the future.

LEON4 SPARC V8 Processor

The LEON4 processor is the fourth generation of processors in the successful LEON processor family, which is targeting embedded and aerospace systems.

LEON4 has all the features of a LEON3 processor, including a SPARC V8 compliant architecture with a seven-stage pipeline for fast and energy-efficient execution, configurable Level 1 (L1) instruction and data caches, configurable number of register windows, and IEEE-754/IEEE-1754 compatible floating-point units. This makes LEON4 software compatible with all the code written for the LEON3 processor.

For improved performance the LEON4 processor includes a branch prediction unit, a wide (64 or 128-bit) processor bus, support for configurable MMU page size, and a Level 2 (L2) cache. These micro-architectural improvements make a LEON4 processor on average 35% faster than a LEON3 processor operating at the same clock frequency.

Branch Prediction

LEON4 includes a branch prediction unit that implements a branch taken policy. This allows the pipeline to continue executing instructions when a branch is encountered in the instruction stream. In previous generations of the LEON processor the pipeline is stalled for one or two clock cycles if the branch condition depends on the result of any of the two instructions executed before the branch. With the branch prediction unit it is not necessary to wait for the branch condition to be evaluated before fetching new instructions.

There is no penalty for miss-speculations. The speculatively fetched instructions are simply flushed from the pipeline and new instructions are fetched from the correct branch target.

MMU Page Size

The LEON4 Memory Management Unit (MMU) can be configured to have a 4, 8, 16, or 32 kbyte page size. A larger page size makes it possible to increase the size of the L1 cache. This is because the L1 cache way size cannot be larger than the page size of the MMU without causing memory aliasing. The support for a configurable MMU page size makes it possible to increase the L1 data and instruction caches to a maximum of 4x32 kbyte for a 4 way cache configuration.

An added advantage of a larger page size is that it increases the Translation Lookaside Buffer (TLB) hit rate. This is due to the fact that since each page is larger there will be fewer pages in total and the TLB entries will represent a larger portion of the memory. One disadvantage with a large page size is that the smallest allocatable memory size is a complete page, e.g. if many small files are to be opened each of these will require a whole page.

Configurable Processor Bus

The AMBA Advanced High-Speed Bus (AHB) of the LEON4 processor is configurable to either 64 or 128 data bits. The wide bus allows LEON4 to fetch a complete L1 cache line in a single data transfer (in the case of a 128-bit wide bus and a 128-bit cache line). This reduces the cache-miss penalty and the bus activity caused by the processor in a SoC design.

Level 2 Cache

An L2 cache is being developed in conjunction with the LEON4 processor. The L2 cache is highly configurable and supports different associativity (1/2/4), way size (1-256 kbyte), and AHB bus width (64 or 128 data bits).

An L2 cache reduces the L1 cache-miss penalty for the LEON4 processor and it reduces the load on off-chip memory. The added advantage of an L2 cache is therefore not only an improvement in performance but also a reduction in energy, since power-dissipating off-chip signaling is reduced.

FPGA Prototype System

A SoC prototype, based on the LEON4 processor and GRLIB, has been developed and functionally verified on Xilinx ML505 and ML507 FPGA boards.

The prototype design consists of the LEON4 processor and a set of IP cores connected through AMBA AHB/APB buses. The complete system can be seen in Figure 1[1].

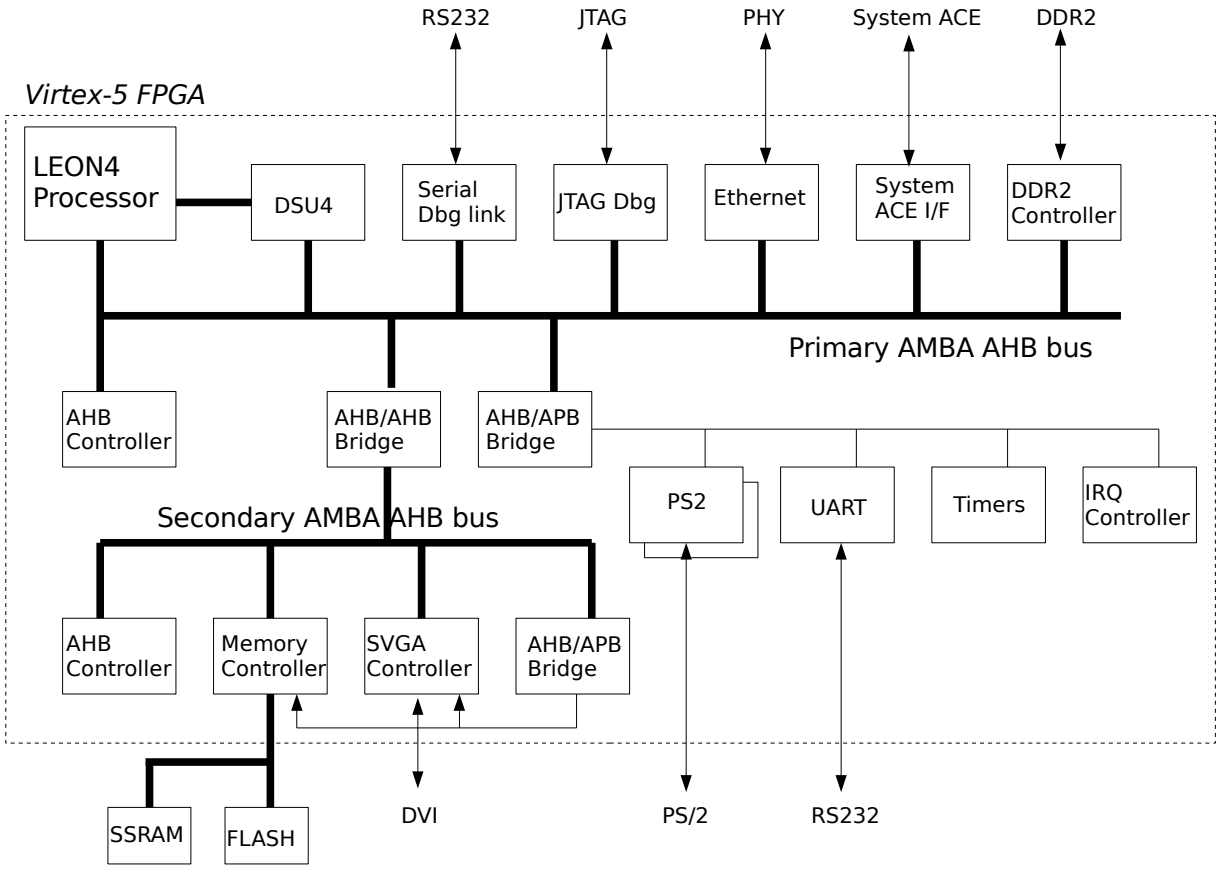

Figure 1: Block diagram of a LEON4 SoC for FPGA prototyping

The prototype design has two AMBA AHB buses, with the LEON4 processor, high-speed interfaces, and debug interfaces being connected to the primary AHB bus and a SVGA controller, a memory controller for Flash PROM and SSRAM, and a local AHB-to-APB bridge connected to the secondary AHB bus. The SSRAM is used as frame buffer for the SVGA controller and the use of a dedicated AHB bus reduces the bandwidth requirements of the main AHB bus. The local AHB-to-APB bridge on the secondary AHB bus is used to access control registers of the SVGA and memory controller. The two AHB buses are connected to each other through an AHB-to-AHB bridge.

A number of low-speed interfaces and IP cores are connected to an APB bus that is connected to the main AHB bus through an unidirectional AHB-to-APB bridge.

1 The block diagram is not a detailed description of the system. Some cores have more than one instance and several cores are connected both to an AHB and an APB bus.

The primary AHB bus is 128 bits wide but it is only the LEON4 processor and DDR2 memory controller that are connected to all 128 data bits. All other cores on the main AHB bus are connected to the 32 least significant data bits of the bus.

The on-chip peripheral devices include an Ethernet 10/100 Mbit MAC, JTAG debug interface, one UART, interrupt controller, timers, System ACE interface, PS/2 interfaces, and an I/O port. The System ACE interface provides a memory mapped interface to the development board's System ACE CompactFlash solution. This allows CompactFlash cards to be used as hard disk storage.

The L2 cache is currently under development and is therefore not part of the current prototype design. The L2 cache development is expected to be completed in summer 2009 and the prototype design will then be updated.

We have Linux running on the prototype design in our labs and all SPEC2000 benchmarks have successfully been executed. The preliminary results show 19.1 SPECint and 12.5 SPECfp at 70 MHz, giving a performance of 0.27 SPECint/MHz and 0.2 SPECfp/MHz.

The LEON4 processor achieves a lower Clocks Per Instruction (CPI) count during heavy loads than a LEON3 processor operating at the same clock frequency. For the SPEC CPU2000 benchmarks the LEON4 processor is 30%-40% faster than the LEON3.

System on Chip ASIC

A customer evaluation SoC ASIC with dual LEON4 cores and numerous high-speed and low-speed interfaces is currently under development. The evaluation SoC has an AMBA AHB bus to which the two LEON4 cores, high-speed interfaces, Debug Support Unit (DSU4), and system debug links are connected. A variety of low speed interfaces are connected to two separate APB buses that are connected to the AHB bus through two AHB-to-APB bridges. In this design the SVGA controller is connected directly to the main AHB bus, since the operating frequency of the AHB bus is high enough to provide the required bandwidth. This simplifies the design compared to the prototype design described in the previous section. The complete system can be seen in Figure 2[2].

2 The block diagram is not a detailed description of the system. Several cores are connected both to the AHB bus and an APB bus.

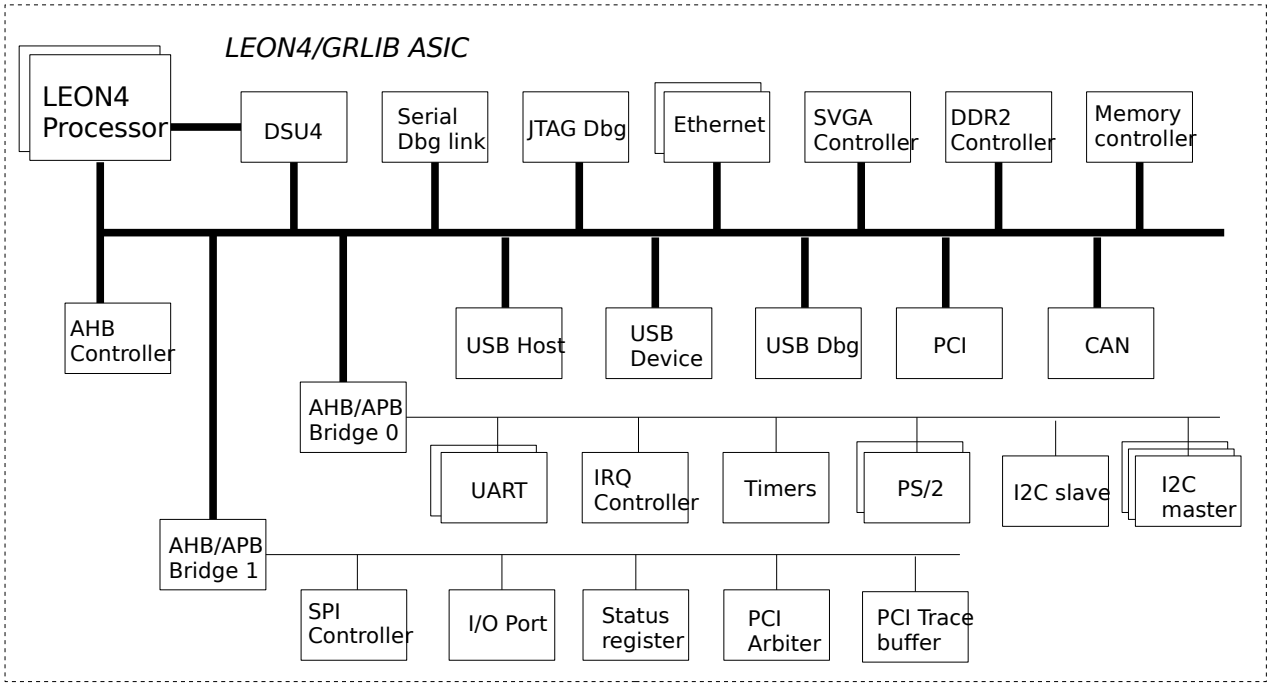

Figure 2: Block diagram of the LEON4 based evaluation SoC ASIC

The evaluation SoC ASIC implements all the main interfaces as expected from a desktop computer, including PCI, dual Ethernet 10/100 Mbit MACs, USB (both host and device), DVI, DDR2, and PS2. This makes the evaluation SoC readily available for development of Linux and PDA like applications. In addition, the evaluation SoC also has a general SPI controller, an SPI memory controller for Flash PROM, three I^2C masters and one slave, two UARTs, and a CAN controller. The SoC is therefore a suitable platform for development of a wide range of embedded applications.

The evaluation SoC will be manufactured in eASIC's 90 nm Nextreme technology and is expected to operate at a core frequency of 200 MHz with a 32-bit wide DDR2 400 MHz memory interface. The DDR2 memory interface is chosen to be 32 bit wide due to pin limitations. Operating the DDR2 interface at twice the frequency of the AHB bus makes it possible to read/write two 32-bit words from/to memory for each AHB bus cycle. It then becomes natural to have a 64-bit wide AHB bus.

The evaluation SoC ASIC and an accompanying development board is expected to be ready for delivery during summer 2009.

Outlook

A fault-tolerant version (LEON4-FT) of the LEON4 processor is being developed and is expected to be available in late 2009 or early 2010. The LEON4-FT will have all the fault-tolerant features of the LEON3-FT processor while incorporating the new features of the LEON4 processor described in this paper.