

Next Generation Multi-Purpose Microprocessor

Jan Andersson, Magnus Sjölander, Jiri Gaisler
Aeroflex Gaisler, Kungsgatan 12, SE-411 91, Göteborg, Sweden,
Tel +46 31 7758650, {jan, magnus, jiri}@gaisler.com

Roland Weigand
European Space Agency, Keplerlaan 1 – PO Box 299, 2220AG Noordwijk ZH,
The Netherlands, +31 71 565 32 98, roland.weigand@esa.int

Extended Abstract

The Next Generation Multi-Purpose Microprocessor (NGMP) is a SPARC V8(E) based multi-core architecture that provides a significant performance increase compared to earlier generations of European space processors. The NGMP is currently developed at Aeroflex Gaisler in Göteborg, Sweden, in an activity initiated by the European Space Agency.

The presentation will describe the baseline architecture, point out key choices that have been made and will also emphasise points that are still open. The software environments and operating systems that will be available for the NGMP, together with a general overview of the new LEON4 microprocessor, will also be presented.

It should be noted that this abstract describes the current state of Aeroflex Gaisler's work on the NGMP. The actual presentation may describe later developments.

Architectural Overview

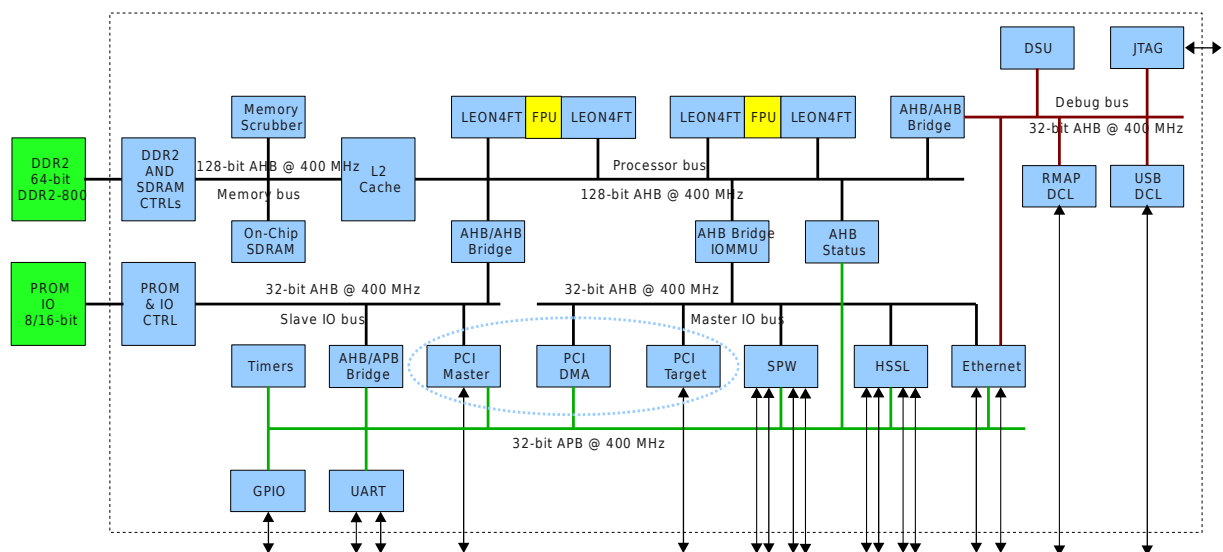


Illustration 1: NGMP Block Diagram

Illustration 1 above depicts an overview of the NGMP architecture. The system will consist of five AHB buses; one 128-bit Processor bus, one 128-bit Memory bus, two 32-bit I/O buses and one 32-bit Debug bus. The Processor bus will include four LEON4FT cores connected to a shared L2 cache. The Memory bus is located between the L2 cache and the main external memory interfaces, DDR2 and SDRAM interfaces on shared pins, and will include a memory scrubber and possibly on-chip memory. As an alternative to a large on-chip memory, part of the L2 cache could be turned into on-chip memory by cache-way disabling. The I/O bus has been split into two separate buses where all slave interfaces have been placed on one of the buses (Slave I/O bus) and all master interfaces have been placed on the other bus (Master I/O bus). The Master I/O bus connects to the Processor bus via an AHB bridge that provides access restriction (IOMMU) functionality.

The two I/O buses include all peripheral units such as PCI, High-Speed Serial Link, Ethernet MAC, and SpaceWire interfaces. The dedicated 32-bit Debug bus connects one debug support unit (DSU), one JTAG debug link, one SpaceWire RMAP target, one USB debug communication link, and optionally two Ethernet debug communication links. The Debug bus allows for non-intrusive debugging through the

DSU and direct access to the complete system, since the Debug bus is not placed behind an AHB bridge with access restriction functionality.

The target frequency of the LEON4FT and on-chip buses is 400 MHz, but depends ultimately on the implementation technology. The SDRAM interface will be able to run at the same or one third of the system frequency. The DDR2 interface will be run at the same or twice the system frequency. The clock scaling factor between the memory interfaces and the rest of the chip is selectable via an external signal.

All I/O master units in the system contain dedicated DMA engines and are controlled by descriptors located in main memory that are set up by the processors. Reception of, for instance, Ethernet and SpaceWire packets will not increase CPU load. The cores will buffer incoming packets and write them to main memory without processor intervention.

The list below summarizes the specification for the NGMP system:

System architecture

- 128-bit Processor AHB bus
 - 4x LEON4FT with 16 + 16 KiB cache, SPARC Reference MMU, physical snooping, 32-bit MUL/DIV and GRFPU shared between pairs of LEON4FT with 4-word instruction FIFO, or (TBD) dedicated GRFPU for each processor core.
 - 1x Shared L2 cache with memory access protection (fence registers)
 - 1x 128-bit to 32-bit unidirectional AHB to AHB bridge (connecting Debug bus with Processor bus)
 - 1x 128-bit to 32-bit unidirectional AHB to AHB bridge (connecting Processor bus to slave IO bus)
 - 1x 32-bit to 128-bit unidirectional AHB to AHB bridge with IOMMU (connecting master IO bus to Processor bus)
- 128-bit Memory AHB bus
 - 1x 64-bit DDR2-800 memory interface with Reed-Solomon ECC (16 or 32 check bits)
 - 1x 64-bit SDRAM PC133 memory interface with Reed-Solomon ECC (16 or 32 check bits)
 - 1x Memory scrubber
 - 1x On-chip SDRAM (if available on the target technology)
- 32-bit Master I/O AHB bus
 - 4x SpaceWire cores with redundant link drivers and RMAP @ 200 Mbit/s
 - 4x High-Speed Serial Link with SpaceFibre interface, if IP's available
 - 2x 10/100/1000 Mbit Ethernet interface with MII/GMII PHY interface
 - 1x 32-bit PCI target interface @ 66 MHz
- 32-bit Slave I/O AHB bus
 - 1x 32-bit PCI master interface @ 66 MHz with DMA controller mapped to the Master I/O bus
 - 1x 8/16-bit PROM/IO controller with BCH ECC
 - 1x 32-bit AHB to APB bridge, connecting 32-bit APB bus:
 - 1x General purpose timer unit
 - 1x 16-bit general purpose I/O port controller
 - 2x 8-bit UART interface
 - 1x Multiprocessor interrupt controller
 - 4x Secondary interrupt controller
 - 1x PCI arbiter with support for four agents
 - 1x AHB status register
 - 1x General Purpose register for clock gating
- 32-bit Debug AHB Bus
 - 1x Debug support unit
 - 1x USB debug link
 - 1x JTAG debug link
 - 1x SpaceWire RMAP target

The fault-tolerance in the NGMP system is aimed at detecting and correcting SEU errors in on-chip and off-chip RAM. The L1 cache and register files in the LEON4FT cores are protected using parity and BCH coding, while the L2 cache will use BCH. External DDR2 memory will be protected using Reed-Solomon coding, while the boot PROM will use BCH. Any RAM blocks in on-chip IP cores will be protected with BCH or TMR. Flip-flops will be protected with SEU-hardened library cells if available, or TMR otherwise.

LEON4 Microprocessor and L2 Cache

The LEON4 processor is the latest processor in the LEON series. LEON4 is a 32-bit processor core conforming to the IEEE-1754 (SPARC V8) architecture. It is designed for embedded applications, combining high performance with low complexity and low power consumption. LEON4 improvements over the LEON3 processor include:

- Branch prediction
- 64-bit pipeline with single cycle load/store
- 128-bit wide L1 cache
- 4-port register file

The LEON4FT processor connects to an AMBA AHB bus with an 128-bit data width. This leads to a 4x performance increase when performing cache line fills. Single cycle load and store instructions increases performance and also take advantage of the wider AHB bus.

Static branch prediction has shown to give an overall performance increase of 10%. The LEON4 also has support for the SPARC V9 compare and swap (CASA) instruction that improves lock handling and performance.

An important factor to high processor performance and good SMP scaling is high memory bandwidth coupled with low latency. An 128-bit AHB bus will therefore be used to connect the LEON4FT processors. This will allow 32 bytes to be read in 2 clocks, not counting the initial memory latency. To mask memory latency, the GRLIB L2 cache will be used as a high-speed buffer between the external memory and the AHB bus. A read hit to the L2 cache typically requires 3 clocks, while a write takes 1 clock. A 32-byte cache line fetch will be performed as a burst of two 128-bit reads. The first read will have a delay of 3 clocks and the second word will be delivered after one additional clock. A cache line will thus be fetched in 4 clocks (3 + 1). Error correction will add an additional latency of 1 clock to all read accesses to allow time for checksum calculation.

Improved Support for Multi-Processor Operation and Debugging

Beyond support for standard SMP configurations, e.g. with a central multi-processor interrupt controller, NGMP will also support ASMP configurations: Per CPU-core dedicated timer units and interrupt controllers allow running separate operating systems on each of the cores. In addition to the MMU's in each of the CPU cores and the IOMMU, memory read/write access protection (fence registers) implemented in the L2 cache also improves the time and space partitioning.

The NGMP platform will include new and improved debug and profiling facilities compared to the LEON2FT and LEON3FT. The debug support features of NGMP include:

- AHB bus trace buffer with filtering and counters for statistics
- Processor instruction trace buffers with filtering
- Performance counters in each processor core
- Dedicated debug communication links that allow non-intrusive accesses to the processors' debug support unit
- Hardware break- and watchpoints
- Monitoring of data areas

Instruction Set Simulator

The instruction set simulator for NGMP will build on the GRSIM multiprocessor simulator. The simulator consists of an AHB bus model with underlying event-driven simulation engine. C-models of IP cores are attached to the AHB model, and linked into a final simulator. The GRSIM library is re-entrant and thread-safe, and allows simulation of any number of buses and IP cores. It is therefore particularly suitable for simulating multi-processor LEON systems such as the NGMP.

GRSIM can be run in stand-alone mode, or connected through a network socket to the GNU GDB debugger. In stand-alone mode, a variety of debugging commands are available to allow manipulation of memory contents and registers, breakpoint/watchpoint insertion and performance measurement. Connected to GDB, GRSIM acts as a remote target and supports all GDB debug requests. The communication between GDB and GRSIM is performed using the GDB extended-remote protocol. Any third-party debugger supporting this protocol can be used.

The overall accuracy will depend on the accuracy of the simulation models for the DDR2 memory controller and the L2 cache. The target is 10 % which is considered challenging but will be the goal during the development.

Software Support

The GRMON debug monitor from Aeroflex Gaisler will be extended to support all new functionality for debugging and profiling that will be included in the NGMP. The hardware platform will provide full backwards compatibility with existing LEON3FT software and all standard compilers that can produce correct SPARC V8 code can be used.

Board support packages for the NGMP will be delivered for the following operating systems:

- RTEMS 4.8 and 4.10
- eCos
- VxWorks 6.7
- Linux 2.6

Conclusion

The NGMP will be a SPARC V8(E) based multi-core architecture, that provides a significant performance increase compared to earlier generations of European space processors, with high-speed interfaces such as SpaceWire and Gigabit Ethernet on-chip. The platform will have improved support for profiling and debugging compared to previous generations of European space processors and will have a rich set of software immediately available due to backwards compatibility with existing SPARC V8 software and LEON3 board support packages.

The NGMP is part of the ESA roadmap for standard microprocessor components. It is developed under ESA contract, and it will be commercialised under fair and equal conditions to all users in the ESA member states. The NGMP is also fully developed with manpower located in Europe, and it only relies on European IP sources. It will therefore not be affected by US export regulations.